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CS-12

00242

ADCA / MCA (III Year)

Term-End Examination

June, 2010

CS-12 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 75*

Note : ***Question no. 1*** *is* ***compulsory.*** *Answer* ***any three*** *questions from the rest.*

1. (a) Explain the significance of Amdahl's law for a multiprocessor system. Also, derive an expression for speedup of an n-processor system. **6**

(b) Consider a cache (M1) and memory (M2) hierarchy with following characteristics : **10**

M1 : 16 K words, 60 ns access time

M2 : 4 M words, 800 ns access time
Assume 8 - word cache blocks and set size of 256 words with set associative mapping.

(i) Show mapping between M1 and M2.

(ii) Calculate the effective memory access time with a cache hit ratio of h = 0.95.

(c) Explain the snoopy bus protocols for bus connected computer systems. 7

(d) What is superpipelined processor ? Discuss the performance of superpipelined design. 1+6

2. (a) Explain a distributed memory multi computer system with the help of an appropriate diagram. 5

(b) Make the data dependency graph of the following code segment : 8

S1 : $A = B + C$

S2 : $D = E \times A$

S3 : $F = G + A$

S4 : $A = H + D$

S5 : $I = E \div C$

(c) Define the cache aliasing problem. 2

3. (a) Differentiate between asynchronous and synchronous pipeline. What causes a processor pipeline to be under pipelined ? 10

(b) Explain the concept of overlapping register window in the SPARC architecture, with the help of a diagram. 5

4. (a) Explain the store-and-forward and wormhole message routing schemes. And also analyse their communication latenciess. **4+4**

(b) With the help of suitable diagram, differentiate between RISC and CISC architectures. **7**

5. Explain ***any three*** of the following : **15**

(a) Perfect shuffle network.

(b) PRAM model of computers.

(c) Buffer and channel deadlocks.

(d) Inverted paging mechanisms.
