ADCA / MCA (III Year)

Term-End Examination

December, 2010

01377

CS-12 : COMPUTER ARCHITECTURE

Time : 3 hours   *Maximum Marks : 75*

Note : Question number 1 is compulsory. Attempt any three from rest.

1. (a) Compare the relative performance of a   6
         superscalar processor with that of a scalar
         base machine.

    (b) A two level memory system has 8 virtual   6
         pages on a disk to be mapped into 4-page
         frame in main memory. The page trace is
         given as :

         2,0,4,4,6,6,3,0,2,6,4,3

         Compute the hit ratio in the main memory
         using LRU replacement policy. Assume the
         page frame initially has 4,2,0,3

    (c) What are the factors which affect cache hit   6
         ratio. Explain through appropriate graphs.

(d) Draw two NUMA models based on a hierarchical cluster approach and shared local memory. Also list the key differences between the two.   6

(e) What are the problems encountered in scaling up a computer to massively parallel system ?   6

2. (a) Explain the VLIW architecture. Explain low pipelining is incorporated in VLIW architecture for a degree m = 3.   7

(b) State the Bernstein's conditions, based on which two processes can execute in parallel. For the following example detect parallelism using Bernstein's conditions :   8

I_1 :   A = B × E

I_2 :   B = D × C

I_3 :   A = D + B

I_4 :   C = F + G

I_5 :   E = G − H

Illustrate various dependencies using dependency graph.

3. (a) Differentiate between write back and write   6
       through cache updation schemes with the
       help of suitable diagrams.

   (b) Explain the functioning of 8×8 omega   6
       network with the help of diagram.

   (c) State Amadhl's law. Expalin its significance.   3

4. (a) Compare the relative merits of the following   10
       cache memory organisations :-

       (i)   Direct mapping cache

       (ii) Set associative cache

       (iii) Fully associative cache

       (iv) Sector mapping cache.

   (b) What is the purpose of prefetch buffers in   5
       instruction pipelining ? What are the other
       kinds of buffers used? Give one application
       each of these buffers.

5. (a) Draw data flow graph of the following   6
       expression evaluation :

       $F = (a-b) * (a+c) / (d-e)$

   (b) What are the factors limiting the degree of   4
       superscalar design.

   (c) What are the differences between string   5
       reduction of graph reduction machines ?

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