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BIELE-011

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00446

June, 2015

BIELE-011 : DIGITAL SYSTEM DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. Explain binary full adder. Draw a 4-bit adder and explain its working. Calculate the delay in generation of final carry. *10*

2. Design a synchronous BCD counter, using S-R Flip-Flops. Give its State diagram and Timing diagram. *10*

3. What is the difference between serial and parallel transfer ? Give the circuit diagram of a register that can be used for serial as well as parallel data transfer under mode control signal. *10*

4. Discuss the principles of controller architecture design in detail along with its timing and frequency consideration. *10*

5. Discuss an example of use of multiplexer in system controller. Explain with the help of a suitable diagram. *10*

6. Write short notes on the following : *2×5=10*

   (a) Cycle and Races in Asynchronous Circuit

   (b) Hazards in Combinational and Sequential Logic Circuits

7. How are asynchronous finite state machines different from synchronous finite state machines ? State the design principles of asynchronous finite state machines. *10*

8. Discuss application of PLAA and FPLA in system controller design. *10*

9. What is meant by operator overloading ? Give an example. When should operator overloading be avoided ? *10*

10. Discuss the different data types and data objects used in VHDL. Write a VHDL program for a 4:1 multiplexer using data flow model. *10*