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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

June, 2015 00656

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

1. What are the basic elements of Hardware Description Language ? Explain them with the help of an example. *5+5=10*

2. Differentiate between DATAFLOW and STRUCTURAL modelling. How does dataflow modelling help in overcoming delays in digital systems ? *4+6=10*

3. Explain the various steps for BEHAVIOURAL modelling technique of digital system design. Explain how structural modelling helps in resolving signal value assignment. *5+5=10*

4. Give an overview of different FPGA architectures and designs used in the digital systems. *10*

5. With the help of a suitable example, differentiate between any ***two*** of the following : *5+5=10*

   (a) Generics and Configurations

   (b) Sub-programs and Overloading

   (c) Packages and Libraries

6. Write an algorithm for the steps involved in the design of Mealy and Moore model of state machine. *10*

7. Write a VHDL program for the following : *5+5=10*

   (a) Full Subtractor

   (b) 3 to 8 Decoder

8. What are the various methods used for the testing of single-stuck faults ? Explain any one method using a suitable example. *10*

9. What are the various classical scan design techniques used for testability ? Explain. *10*

10. Write short notes on any ***two*** of the following : *5+5=10*

    (a) Fault Equivalence

    (b) Bridging Faults

    (c) Boundary Scan Standards

    (d) Complex Signal Assignments
