MCA (Revised) / BCA (Revised)
Term-End Examination
June, 2021

MCS-012 : COMPUTER ORGANISATION AND ASSEMBLY LANGUAGE PROGRAMMING

Time : 3 hours *Maximum Marks : 100*

(Weightage : 75%)

Note : *Question number **1** is **compulsory** and carries 40 marks. Attempt any **three** questions from the rest.*

1. (a) Perform the following computations using *signed 1's complement* notation of length 8 bits. Also indicate overflow, if any : *6*

(i) – 76 – 52

(ii) + 79 + 49

(iii) + 79 – 86

(b) Design a full-adder circuit using K-map. *4*

(c) Explain the two-way set associative cache mapping scheme with the help of an example. *5*

(d) What is DMA ? Why is it useful ? Draw the block diagram of a DMA interface. *5*

(e) Instructions of machine are such that they have two register operands. However, to load a register a special instruction has been designed which either contains the operand value or address of the operand. List and explain four addressing modes for this machine. *4*

(f) What is the role of control memory in a micro-programmed control unit ? Explain the organisation of control memory with the help of a diagram. What is a horizontal micro-instruction ? Explain. *6*

(g) Write a program using 8086 assembly language that moves content of byte memory location X1 and X2 to AL and BL registers. The program then finds the larger value of AL or BL register and stores it in DL register. *6*

(h) Assume the following values in the registers :
Instruction Pointer (IP) contains $(A521)_h$
Stack Pointer (SP) contains $(OOFF)_h$
Code Segment (CS) contains $(OFFF)_h$
Stack Segment (SS) contains $(OOOF)_h$
Find the following using the above information : *4*

(i) Physical address of top of stack

(ii) Physical address of instruction

2. (a) Draw logic diagram to implement AND, OR and NOT operations using NAND gate(s). *5*

(b) Explain the following in the context of floating point number representation with the help of an example : *5*

(i) Normalised mantissa

(ii) Biased exponent

(c) How many RAM chips of size 512 K $\times$ 1 bit are required to build 1 MB memory ? *2*

(d) What is Programmed Input/Output ? Explain with the help of a diagram. Explain the difference between Programmed I/O and Interrupt driven I/O. *6*

(e) What is Latency time in the hard disk ? *2*

3. (a) Explain the steps required to fetch an instruction from a memory location to instruction register with the help of micro-operations. *5*

(b) What will be the length of various fields of an instruction considering the following ? *5*

(i) 64 possible operations

(ii) 8 addressing modes

(iii) Memory size of 4 KB (byte addressing is used)

(iv) It has 32 registers

(v) Each instruction has one register and one memory operand

Make suitable assumptions.

(c) Explain the concept of NEAR and FAR procedural calls in 8086 microprocessor with the help of one example each. *6*

(d) Explain the use of INT 21h in 8086 microprocessor for reading a single character from the keyboard with the help of an example. *4*

4. (a) Draw and explain the truth table and logic diagram of a 3-bit synchronous counter. *5*

(b) Explain the von Neumann architecture with the help of a diagram. *5*

(c) What is an Input/Output processor ? How is it different from DMA ? *4*

(d) Differentiate between the following : *6*

(i) SRAM and DRAM

(ii) ROM and Flash Memory

5. (a) What is the use of stack in subroutine CALL instruction ? Explain using an example. *5*

(b) Why is RAID used in computers ? What is RAID Level 0 ? *3*

(c) Explain the following assembly language instructions with the help of an example each : *8*

(i) MUL

(ii) ADD

(iii) TEST

(iv) SHR

(d) Explain the use of CX register in implementing looping in 8086 assembly language. *4*