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BIELE-012

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00016

Term-End Examination

June, 2016

BIELE-012 : ELECTRONIC SWITCHING CIRCUITS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Assume missing data, if any. Use of scientific calculator is permitted.*

1. (a) Show how a J-K flip-flop can be converted into a D flip-flop. Explain the change in behaviour by analysing its gate equivalent circuit. *6*

(b) Give the classification of sequential circuits. *4*

2. A sequential circuit has two D flip-flops, A and B, two inputs, x and y, and one output, z. The flip-flop input equations and circuits output are as follows :

$$D_A = x'y + xA, \quad D_B = x'B + xA, \quad z = B$$

(a) Draw the logic diagram of the circuit.

(b) Tabulate the state table. *10*

3. Design a two-input, two-output synchronous sequential circuit, which produces an output z = 1 whenever any of the following input sequences occur : 1100, 1010 and 1001. The circuit resets to its initial state after a '1' output has been generated.

(a) Form the state diagram and state table.

(b) Draw the logic circuit. *10*

4. (a) Determine the conditions under which two equivalent machines are isomorphic. *4*

(b) Prove that, to every q-output, n-state Mealy Machine, there corresponds a q-output Moore Machine which accepts exactly the same sequences and has no more, than qn+1 states. *6*

5. For the flow table given below, determine all the essential output hazards and essential internal variable hazards. *10*

State, output			
$x_1 x_2$			
00	01	11	10
①,1	2, 0	3, 1	⑤, 1
4, 0	②, 0	3, 1	8, 1
4, 0	7, 0	③, 1	8, 0
④,0	6, 1	9, 0	⑧, 0
4, 0	⑥, 1	9, 1	5, 1
1, 0	⑦, 0	⑨, 1	5, 1

6. A memory device has two binary inputs, Y_1 and Y_2, and three binary outputs y_1, y_2 and y_3. When Y_1 is pulse, both y_1 and y_2 are complemented. It is not allowed to pulse Y_1 and Y_2 simultaneously. Use one such device to realize pulse sequential circuit shown in the table. *10*

PS	NS		Z
	x_1	x_2	
A	D	A	0
B	C	D	0
C	A	B	0
D	B	B	1

7. Prove that if a circuit is designed, so that it is hazard-free in its tie-sets, then it is also hazard-free in its cut-sets. *10*

8. Briefly discuss how the static hazards are produced in combinational circuits. How can they be eliminated ? *10*

9. Briefly discuss symmetric functions. List all the properties of symmetric functions. *10*

10. Write notes on any ***two*** of the following : *2×5=10*

    (a) Contact Network

    (b) Identification of Symmetric Functions

    (c) Sequence generator for generating the sequence 01100
