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BIELE-011

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00566

Term-End Examination

June, 2016

BIELE-011 : DIGITAL SYSTEM DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Use of scientific calculator is allowed.*

1. Minimise the Boolean function $f(x_1, x_2, x_3, x_4, x_5) = \sum m(0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)$ by using the tabular method. Show all prime implicants and essential prime implicants. *10*

2. Discuss the working of a Johnson ring counter (4 bit). Design the same by using J-K flip-flop. State the steps/sequences it will go through, when it is loaded with initial value 1010. *10*

3. Describe the process of controller and data path design with its block diagram and logic diagram. *10*

4. Design a 32×1 multiplexer by using 2×1 MUX only. How many numbers of 16×1 MUX are required to have a 256×1 MUX ? *10*

5. What is an instruction set ? Explain programmable controller with fixed instruction set with subroutine capability. *10*

6. (a) Design a ripple 3-bit down counter by using T flip-flop. *5*

   (b) Explain about the race around condition and the remedy to overcome it. *5*

7. Write a data flow description for a 4-bit full adder. Include initial carry also. *10*

8. Design an asynchronous counter that counts the sequence 0, 1, 2, 4, 6, 5, 7 and repeats by using J-K flip-flop. *10*

9. (a) A binary counter is required to count up to 16383_{10}. How many flip-flops are required ? If the input clock frequency is 10·5 MHz, what is the frequency of the MSB output ? *5*

   (b) Write the Boolean expression for a 3-bit comparator to produce A > B, A < B and A = B conditions. *5*