No. of Printed Pages : 3

BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00296

June, 2016

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

1. With sample waveforms, explain the transport delay and inertial delay in digital circuits. *10*

2. Explain structural modelling with an example. Write a VHDL program for detecting the number of 1's in an eight-bit vector, if even number of 1's output = '0' and if odd number of 1's output = '1'. *10*

3. (a) With suitable examples, compare variables and signals in VHDL. 5

(b) Define Generics. Using Generics statement, write a VHDL code for a three input NAND gate. 5

4. (a) Write a VHDL code for the synthesis of a case statement. 5

(b) Explain simulation semantics. 5

5. (a) What is a subprogram ? How is it used in VHDL programs ? Explain with suitable example. 5

(b) What are the real defects in digital circuits ? Write down the equivalence rules for AND, OR, NAND and NOR gates. 5

6. What are the main reasons of IC malfunction (faults) ? Explain the various types of faults found in digital circuits with suitable examples. 10

7. Give an algorithm for testing of bridging faults. What are the main consequences of bridging faults in digital circuits ? 10

8. (a) Draw and explain Built-In Self-Test (BIST) implementation using Built-In Logic Block Observers (BILBOs). *5*

(b) Discuss the various hardware pattern generation approaches of BIST. *5*

9. What is boundary scan ? Draw and explain the test pattern generator block diagram. *10*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) Packages and Libraries

(b) State machine modelling using VHDL

(c) Testing for single stuck faults