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BIELE-007

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00115

Term-End Examination

June, 2014

BIELE-007 : NANO-ELECTRONICS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. Describe quantum wires and quantum dots with their structural detail and applications. *10*

2. What are the short-channel effects in MOSFET ? Explain the MOSFET device performance with I-V characteristics at nanoscale. *10*

3. What is lithography ? Explain the challenges faced to implement lithography process at nanoscale for MOSFET design. *10*

4. Explain the strained-Si n-MOS transistor with schematic diagram. State the major advantages of strained-Si based MOS transistor. *10*

5. Explain the structure of resonant tunneling diode with its high frequency performance in detail. *10*

6. Describe the high speed Si-Ge hetero-structure bipolar transistor and also explain the trade-off between its current gain and speed. *10*

7. Explain the structural detail of carbon nano-field effect transistor with its I-V characteristics and usefulness in nanotechnology. *10*

8. Draw the structure of spin polarised FET and discuss the difference between I-V characteristics of spin polarised FET with n-channel MOSFET. *10*

9. Discuss the importance of nano-electronics and explain the 'top down' and 'bottom up' approaches of designing nano-electronics devices. *10*

10. Explain the Coulomb Blockade theory in context of single electron transistor with equivalent representation of its I-V characteristics. *10*