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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00628

June, 2014

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. Assume suitable data if missing. All questions carry equal marks.*

1. Compare Top to down and Bottom up design methodology approach. *10*

2. Write a VHDL program for a 4-bit magnitude comparator by Behavioural style of modelling. *10*

3. What is a Testbench and what is the relation of a design entity to its testbench ? Can the same testbench be used for each of the three kinds of simulations ? *5+5=10*

4. What is a component in VHDL ? What does binding mean in terms of components and design entities ? What is the default binding rule for components ? *3+3+4=10*

5. Explain the following based on VHDL programming language : *4+6=10*

   (a) Package

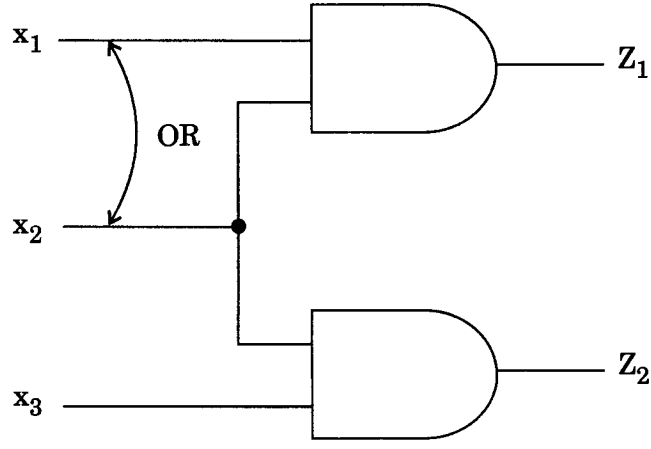
   (b) Generics and Configurations

6. (a) What do you understand by fault masking ? Explain with example. *5*

   (b) Explain the fault equivalence with suitable example. *5*

7. What do you understand by design for testability ? Also explain controllability and observability. *10*

8. In the following circuit let f be the OR bridging fault between x_1 and x_2. This fault changes the functions realized by two outputs Z_1 and Z_2. Give the test vectors that can detect the fault. *10*



9. Draw the boundary scan cell. Also explain various modes of operation associated with it. *4+6=10*

10. Give the classification of Built-in self-test and explain each. *10*