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BIELE-002

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00565

June, 2014

BIELE-002 : MICROELECTRONICS TECHNOLOGY

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. Assume suitable missing data, if any.*

1. (a) Explain the float zone process of crystal growth. How is it different from CZ-technique ?

(b) What is silicon shaping ? How are ingots evaluated ? *2×5=10*

2. Explain the basic transport mechanism and reaction kinetics of vapour-phase epitaxy process showing its various reactors. *10*

3. (a) What is the difference between dry oxidation and wet oxidation ?

(b) Show that 0·44 d_0 thickness of Si is consumed, when SiO_2 is grown over Si. *2×5=10*

4. (a) What is the difference between positive and negative photo resist ?

(b) Discus electron beam lithography process with suitable diagram. *2×5=10*

5. (a) What is the need of plasma in etching process ? How is it created ?

(b) Explain the various properties of etching process. *2×5=10*

6. What is diffusion ? Explain its transport mechanism by deriving the expressions of concentration gradients for the erfc and Gaussian distributions. *10*

7. (a) Explain the basic theory of ion implantation.

(b) What is annealing ? What are the types of annealing used ? *2×5=10*

8. (a) Calculate the RC time constant for a 1 cm long doped poly-silicon inter-connection runner on 1 μm thick SiO_2. The poly-silicon has a thickness of 5000 Å and a resistivity of 1000 μΩ-cm, where $\varepsilon_{Si} = 11{\cdot}7\varepsilon_0$ and $\varepsilon_{SiO_2} = 3{\cdot}97\ \varepsilon_0$.

(b) What is the difference between PVD and CVD ? *2×5=10*

9. (a) Draw the fabrication process sequence of CMOS IC using p-tub, n-tub and twin-tub process.

(b) What is latch-up in CMOS IC's ? How can it be avoided ? *2×5=10*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) RIBE

(b) Silicon on Sapphire

(c) Electromigration
