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BIELE-011

B.TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

June, 2013

BIELE-011 : DIGITAL SYSTEM DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **any five** questions. All questions carry **equal** marks.*

1. (a) With a neat block diagram and functional tables, explain the operation of serial adder with accumulator. **10**

   (b) What is Digital Design concept ? **4**

2. (a) Differentiate between PAL and PLAs. Implement following functions, using a suitable PLA : **10**

   $F_1(A, B, C, D)=\sum m\ (2,3,5,7,8,9,10,11,13,15)$

   $F_2(A, B, C, D)=\sum m\ (2,3,5,6,7,10,11,14,15)$

   $F_3(A, B, C, D)=\sum m\ (6,7,8,9,13,14,15)$

   (b) Give applications of ROM and PROM. **4**

3. (a) Write a VHDL program for the function $Y = AB + C\overline{D}$ using 10
   (i) Behavioral modelling
   (ii) Structural modelling
   (b) What do you mean by Event and Transaction ? Give suitable example. 4

4. (a) Design a 3 digit BCD to binary converter. Draw the block diagram and the state diagram. 10
   (b) Design a 2 bit × 2 bit multiplier using address and gates. 4

5. (a) Using MSI Decoder design a LST circuits. 10
   (b) Write application of 8 × 02 in system control design. 4

6. (a) Explain operator overloading with examples. 10
   (b) Draw hazards excitation map by MEV method. 4

7. Write short notes on *any four* of the following : 3½x4=14
   (a) Fundamental of sequential machine
   (b) Signal attributes
   (c) Signal assignments
   (d) FDLA
   (e) DFD