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BIELE-006

01120

DIPLOMA IN ECE ENGINEERING

Term-End Examination

June, 2013

BIELE-006 : ELECTRONIC PRODUCT DESIGN

Time : 2 hours *Maximum Marks : 70*

Note : *(i) Attempt **any five** questions in all.*
*(ii) Question no. **1** is **compulsory**.*

1. (a) What's the need of regulated dc power supply ? **7x2=14**

(b) List the specifications of input power.

(c) Define Moore and Mealy machines.

(d) List the merits of ASM over FSM.

(e) Draw Bandpass filter response and brief it.

(f) Explain Pole, zero and order of a filter.

(g) Define data acquisition system.

2. Explain combinational and sequential circuit design with suitable examples. **14**

3. (a) Design a combinational circuit using ROM, which accepts a 3 bit number and generates an output binary number equal to the square of input number. **7**

(b) Compare FSM and ASM. Also explain features of ASM. **7**

4. Design a sequence detector which generates an output $z = 1$, whenever the string is 0110 and generates a 0 at all other times. Implement the circuit using D flip flops. Overlapping is allowed. **14**

5. (a) Show that any second order KRC filter, in which K appears only in the s-term in denominator has always $S_k^a > 2a - 1$. **7**

   (b) Design a Cauer low pass filter with $f_C = 1KH_Z$, $fs = 1.3KH_Z$, $A_{max} = 0.1$ dB, $A_{min.} = 40$ dB and dc gain $H_O = 0$ dB. **7**

6. Explain the concept of cascading of filters to design higher order filters, with the help of an example. **14**

7. Explain the interfacing of Relay, Display and DAC with PWM for analog output in data acquisition system. **14**

8. Write short note on ***any four*** : **3½x4=14**
   (a) Mealy and Moorey Models.
   (b) Indicator for over voltage and current.
   (c) ASM technique.
   (d) D Flip Flop versus T Flip Flop.
   (e) Frequency Response Simulation.
   (f) Analog Signal Conditioning System.