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BIELE-003

B.TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00810

Term-End Examination

June, 2013

BIELE-003 : MODELING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *(i) Attempt any **seven** questions.*

(ii) Assume suitable missing data if any.

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1. (a) Discuss the role of HDLs in semiconductor industry. Mention different HDLs available in market. 5

   (b) Explain EDA tools used for design. 5

2. Explain data objects and data types in detail. 10

3. Explain generics and configurations. Why these are used ? 10

4. Write a VHDL program for four bit shift register, using behavioural modelling. 10

5. (a) Explain inertial and transport delay with the help of suitable example. 5

   (b) Consider a gate level implementation of full adder. Design an economical test plan to test this full adder circuit. 5

6. Analyze the equivalency of stuck at faults in an AND-OR circuit implementing XOR function and identify the minimum number of tests detecting all testable faults. 10

7. Define controllability and observability and explain random test generation method. 10

8. Explain classical scan designs and boundary scan standards in detail. 10

9. With the help of suitable example, explain test pattern generation for Built in self test architecture. 10

10. Write short notes on **any two** : 5x2=10
    (a) Resolved signal values.
    (b) Design flow for circuit design.
    (c) Design system testing issues.