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BIEL-030

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DIPLOMA VIEP ELECTRONICS AND COMMUNICATION ENGINEERING (DECVI)/ ADVANCED LEVEL CERTIFICATE COURSE IN ELECTRONICS AND COMMUNICATION ENGINEERING (ACECVI)

Term-End Examination

June, 2013

BIEL-030 : DIGITAL ELECTRONICS

Time : 2 hours *Maximum Marks : 70*

Note : *(i) Attempt **any five** questions. Each question carries **equal** marks.*

*(ii) Question no **one** is compulsory (objectives).*

(iii) All the questions are to be answered in English Language only

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1. Attempt all objective questions. **7x2=14**

(a) A 4-bit binary number whose 2'S compliment is also same is :

(i) 0 0 0 1 (ii) 0 1 0 1

(iii) 0 1 1 1 (iv) 1 0 0 0

(b) $A + \overline{A} =$ _____.

(i) 0 (ii) 1 (iii) A (iv) $\overline{A}$

(c) A demultiplexer is represented by :

(i) $2^n \times 1$ (ii) $2^n \times n$

(iii) $n \times 2^n$ (iv) 1×2^n

(d) Which has the highest power dissipation Per gate.

(i) TTL (ii) CMOS

(iii) ECL (iv) PMOS

(e) In a left shift register, shifting a bit by one means :

(i) division by 2

(ii) Multiplication by 2

(iii) Subtraction of 2

(iv) Addition of 2

(f) A XOR gate has inputs A and B and output Y. Then the output equation is :

(i) $Y = A\overline{B} + AB$ (ii) $Y = AB + \overline{A}B$

(iii) $Y = \overline{A}\,\overline{B} + AB$ (iv) $\overline{A}B + A\overline{B}$

(g) Which is known as Flash converter.

(i) Weighted resistor D/A converter

(ii) Parallel A/D converter

(iii) Stair step A/B converter

(iv) Up-down counter type A/D converter.

2. (a) Give the binary, BCD, excess - 3, gray code, Hexadecimal and octal representations of decimal numbers 5, and 8. **2x7=14**

(b) Design a binary to gray converter circuit of 3 - bit (variable) ?

3. (a) Simplify the given boolean Function using k-map and implement the minimized expression using Logic gates. 2x7=14

$f(A, B, C, D) = \sum m\ (1, 2, 9, 10, 11, 14, 15)$

(b) Using NAND gate implement OR, AND, XOR and XNOR gates.

4. (a) Implement 8:1 Multiplexer using 4:1 Multiplexer and explain its operation. 2x7=14

(b) Design and implement MOD-5 synchronous counter using J - K Flip Flop.

5. (a) With a neat diagram explain the operation of 4 - bit PISO (Parallel Input Serial Output) shift register. 2x7=14

(b) Draw the truth table of two input NAND gate and NOR gate and implement them using CMOS Logic.

6. (a) Explain the operation of a Master slave J - K flip Flop and show how the race around condition is eliminated. 2x7=14

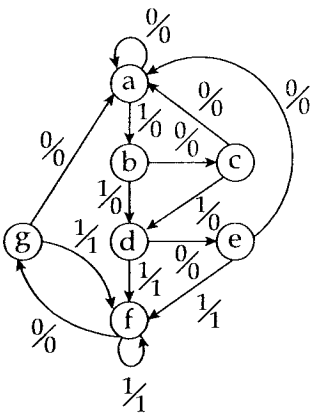
(b) Differentiate between SRAM and DRAM.

7. (a) Convert the following functions to canonical Form : 2x7=14

(i) $y = A + BC + ABC$

(ii) $y = (A + B)\ (\overline{B} + C)$

(b) Obtain the reduced state table and reduced state diagram for a sequential circuit whose state diagram is shown in figure.



8. Write short notes on **any four.** **3.5x4=14**

(a) Propagation delay and fan in and Fan out.

(b) EPROM and EEPROM

(c) ECL Logic family

(d) BCD Arithmatic

(e) Excitation table of Flip Flops.

(f) Boolean Algebra - Basic - Laws