No. of Printed Pages : 4

BIEL-025

00470

B.Tech. in Electronics and Communication Engineering (BTECVI)

Term-End Examination

June, 2013

BIEL-025 : ADVANCE MICROPROCESSOR AND ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *(i) Attempt **any seven** questions.*

*(ii) All questions carry **equal** marks.*

*(iii) Use of **Scientific** calculator is **allowed**.*

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1. Consider the following register transfer statements for two 4 - bit registers R_1 and R_2. **10**

$xT : R_1 \leftarrow R_1 + R_2$

$xT : R_1 \leftarrow R_2$

Every time that variable $T = 1$, either the content of R_2 is added to the content of R_2 is added to the content of R_1 y $x = 1$, or the content of R_2 is transferred to R_1 if $x = 0$. Draw the diagram showing the hardware implementation of the two statements and explain it.

2. How many types of control organizations are there ? Which one is most beneficial for computer system and why ? **10**

3. Analyze the data dependencies among the following statements in a given program : **10**

S_1 : Load R_1, A $/R_1 \leftarrow$ memory (A)/

S_2 : Add R_2, R_1 $/R_2 \leftarrow (R_1) + (R_2)/$

S_3 : Move R_1, R_3 $/R_1 \leftarrow (R_3)/$

S_4 : Store B, R_1 /memory (B) $\leftarrow (R_1)/$

(a) Draw a dependence graph to show all the dependencies.

(b) Are there any resource dependencies if one copy of each functional unit is available in CPU ?

(c) Repeat the above for the following program statements ?

S_1 : Load R_1, M (100) $/R_1 \leftarrow$ memory (100)/

S_2 : More R_2, R_1 $/R_2 \leftarrow (R_1)$ /

S_3 : Inc R_1 $/R_1 \leftarrow (R_1)+1/$

S_4 : Add R_2,R_1 $/(R_2) \leftarrow (R_2)+(R_1)/$

S_5 : Store M (100), R_1 /Memory (100) $\leftarrow (R_1)/$

4. Explain the design space of Advanced Processor Technology. Also explain the concept of Instruction pipelines. **10**

5. Explain the structure and operational requirements of the instruction pipelines used in VLIW processors. Comment on the cycles per instruction expected from this architecture. **10**

6. Explain the inclusion property and data transfer between adjacent levels of a memory hierarchy. Also explain the concept of locality of reference. 10

7. Consider a cache (M_1) and memory (M_2) hierarchy with following characteristics : 10

M_1 : 16 K words, 50 ns access time

M_2 : 1 M words, 400 ns access time

Assuming eight word cache blocks and a set size of 256 words with set-associative mapping.

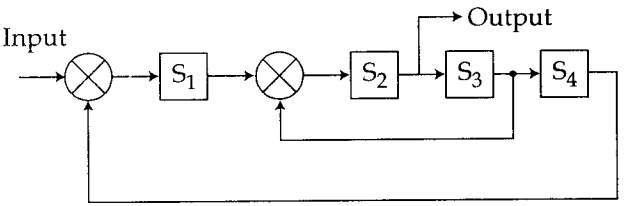
(a) Show the mapping between M_2 and M_1

(b) Calculate the effective memory access time with a cache hit ratio of n = 0.95

8. Prove the lower bound and upper bound on Minimal Average Latency (MAL) is maximum number of checkmarks in any row or equal to the average latency of any greedy cycles and the average latency of any greedy cycle by the number of 1's in the initial collision vector plus 1 respectively. 10

9. Describe the daisy-chaining and the distributed arbites for bus arbitration in a multiprocessor system. State the advantages and short comings of each case from both the implementational and operational points of view. 10

10. Consider the following pipelined processor with four stages. This pipeline has a total evaluation time of six clock cycles. All successor stages must be used after each clock cycles. 10



(a) Specify the reservation table for the pipeline with six columns and four rows.

(b) List the set of forbidden latencies between task initiations.

(c) Draw the state diagram which shows all possible latency cycles.

(d) List all greedy cycles from the state diagram

(e) What is the value of the minimal average latency ?

(f) What is the maximal throughput of this pipeline ?