No. of Printed Pages : **3**

BIEL-003

00141

B.TECH. ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

June, 2013

BIEL-003 : DIGITAL ELECTRONICS

Time : 3 hours *Maximum Marks : 70*

*Note : Attempt **seven** questions in all. All the questions to be answered in English-language only.*

1. (a) Subtract using r's complement 5

$(0.1101)_2 - (111.01)_2$

(b) Convert the BCD number (011110010001) to its decimal equivalent. 5

2. (a) Proof of De-Morgan's theorem using Truth table. 5

(b) Simplify using k-map the given function. 5

$F(A, B, C, D) = \pi M (0, 3, 5, 11, 13, 14, 15) + d (7, 8, 9, 12)$

3. (a) Design 4 bit Gray to Binary code converter using 1:16 demultiplexer (with active low output). 5

(b) Design 4:16 line decoder using 3:8 decoders. 5

4. (a) Realise the function using 16:1 MUX 5

$f(w, x, y, z) = \sum m(0, 3, 4, 7, 9, 13, 15)$

(b) Combinational circuit is defined by the function 5

$F_1(A, B, C) = \sum (3, 5, 6, 7)$

$F_2(A, B, C) = \sum (0, 2, 4, 7)$

implement the circuit with PLA.

5. (a) Draw ASM chart for 2-bit down counter having one enable input x, count is enabled if $x = 0$ and disable if $x = 1$. 5

(b) Design a MOD-5 counter of states (0, 3, 4, 6, 7). Ensure that all unused states reset to zero automatically. 5

6. (a) Draw the logic diagram of D flip-flop and write characteristic table. 5

(b) Draw the logic diagram of T flip-flop and write excitation table. 5

7. (a) Construct 16×8 RAM memory using 16×4 RAM memory ICs. 5

(b) Design a BCD to Excess-3 code converter using PLA. 5

8. (a) Design MOD-10/ Decode/BCD synchronous counter using J - K flip flop. 5

(b) What happens if any input of TTL circuit is kept floating ? 5

9.	(a)	Design a BCD to seven segment decoder using PROM.	5
	(b)	Design a BCD to seven segment decoder using PLA.	5
10.	(a)	Write a short note on Gray Code.	5
	(b)	Write a short note on Excess-3 Code.	5