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BICS-022

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B.TECH. COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

Term-End Examination

June, 2013

BICS-022 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

*Note : Attempt **any seven** questions.*
*All questions carry **equal** marks.*

1. (a) What is cache coherence, and why it is important in shared - memory multiprocessor system ? 6

   (b) How many switch points are there in a crossbar switch network that connects p processors to m memory modules ? 4

2. Show how a compiler would schedule the sequence of any operations for execution on a VLIW processor with 3 execution units. 10

3. (a) Describe the various types of parallel architecture. 5

   (b) Differentiate between RISC and CISC instruction sets. 5

4. (a) What is hit ratio ? Discuss any method to reduce cache misses. 5

(b) Discuss the hazards associated with pipelining. 5

5. Show with timing diagrams instances of synchronous bus output to a slave from a bus master. 10

6. (a) What is the advantage of using interrupt initiated data transfer over transfer under program control without an interrupt ? 5

(b) Why does unrolling a loop often improve performance ? 5

7. (a) Give two advantages of GPR organizations over stack - based organizations. 4

(b) Why do systems that use demand paging generally deliver higher performance than those that use virtual memory ? 6

8. (a) Discuss the difference between tightly coupled multiprocessors with loosely coupled multiprocessors 5

(b) List the various memory issues in multicore processor based systems. 5

9. (a) Why is the data transfer slow in RAID level 6 scheme ? 5

(b) Why does a hypercube 64 processor network use a snoopy bus protocol and a 64 processor multistage network, a directory based protocol ? 5

10. (a) What are the advantages of using a standard input / output bus in a design, as opposed to a direct connection between the processor and each input/ output device ? 7

(b) Explain daisy chain method used in bus arbitration. 3