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BIEL-030

00295

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING (DECVI)/ ADVANCED LEVEL CERTIFICATE COURSE IN ELECTRONICS AND COMMUNICATION ENGINEERING (ACECVI)

Term-End Examination

June, 2012

BIEL-030 : Digital Electronics

Time : 2 hours *Maximum Marks : 70*

Note : *Attempt **any five** Questions. Question **No. 1** is compulsory. Each question carry **equal** marks.*

Attempt all the multiple choice and **True/false** questions.

1. (a) Which of the following code is the example of self complementry code : **2x7=14**

(i) Excess - 3 (ii) BCD

(iii) ASCII (iv) Graycode

(b) Dual of the expression $A.\overline{B}+\overline{C}.D$ is :

(i) $\left(\overline{A}\ B\right)\ \left(C\ \overline{D}\right)$

(ii) $\left(A+\overline{B}\right).\left(\overline{C}+D\right)$

(iii) $(A+B)\ (C+D)$

(iv) None of the above

(c) Expression of sum (S) and carry (C_0) for full adder is :

(i) $S = A \oplus B \oplus C$ $C_0 = AB + BC_{in} + AC_{in}$

(ii) $S = A.B.C$ $C_0 = AB + BC_{in}$

(iii) $S = AB + C$ $C_0 = ABC_{in} + C_{in}B$

(iv) None of these

(d) How many flipflop are required for MOD 6 counter :

(i) > 2 (ii) 3

(iii) 4 (iv) 5

(e) In Moore Model the final output depends only on the present state of memory Element. (T/F)

(f) Adder is an example of sequential circuit. (T/F)

(g) CMOS is slower than TTL (T/F)

2. (a) Prove the following : 7

(i) $A \oplus B = \overline{A} \oplus \overline{B}$

(ii) $B \oplus (B \oplus A.C) = AC$

(b) Convert given base - 7 Number $(35614)_7$ into base 12. 7

3. Minimize following boolean function using K - map and implement logic circuit. 7+7=14

(a) f (A, B, C, D) = m{0, 3, 5, 6, 9, 10, 12, 15} Using NOR gate

(b) f (A, B, C, D) = m {0, 1, 5, 7, 9, 14, 15} + d {2, 6, 8} using NAND gate only.

4. What is multiplexer ? What are the application of multiplexer ? Draw 16 : 1 multiplexer using 4 : 1 multiplexer. **14**

5. Draw the logic diagram of the following flipflops. Also construct the excitation table, characteric equation of each. **14**

   (a) Clocked SR flipflop, JK flipflop, T flipflop

   (b) D flipflop and master slave flipflop.

6. For the state diagram shown in **Fig 1.** obtain the state table and design the circuit using minimum number of T flip flop. **14**

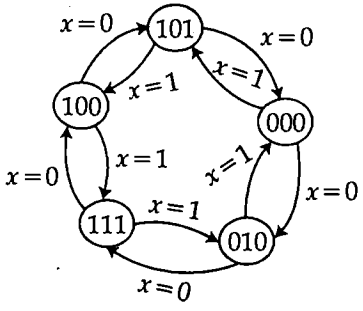

Fig. 1

7. (a) What is meant by open collector output of TTL gate ? What is its utility ? Draw and explain the open collector output and pull up register. **7**

   (b) Draw and Explain CMOS, NOR and NAND gate diagram. **7**

8. Write short note on any four of the following : **3.5x4=14**

(a) All 4 bit shift registers

(b) Steps to design decade asynchronous counter.

(c) Expansion of Memory

(d) Full adder and full subtractor.

(e) D/A converter and A/D converter

(f) Difference between Moore and Mealy M/Cs.