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BIEL-012

00326

B.Tech in Electronics and Communication Engineering (BTECVI)

Term-End Examination

June, 2012

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **any seven** Questions. Each Question carries **10** marks.*

1. Explain the phenomenon of level shifting using P-channel source followers. **10**

2. What are the various types of Digital - to - Analog converter (DAC) ? Explain any one DAC with suitable diagram. **10**

3. With the help of neat sketch explain Analog Multipliers. **10**

4. Find the resolution for a DAC if the output voltage is desired to change in 1 mv increments while using a reference voltage of 5V. **10**

5. Explain about the Decimating filters for ADC's. **10**

6. Design a CMOS logic gate that provides the function. **10**

$$\text{Out} = \overline{x.(y.z+z.w)}$$

Then perform the basic layout of circuit.

7. Discuss in detail the structure of a Multiplying Quad. **10**

8. Explain the basic CMOS OP - amp Design. **10**

9. Find the maximum resolutuion of an ADC which has aperture uncertainity equal to 0.5 n sec. The circuit is sampling a sinusoidal input signal that could be described as : **10**

$$V_{IN} = A \sin 2\pi ft$$

Where A = 2V and f = 100KHz. Also, find the maximum sampling error. The ADC maintains a sampling error less than ½ LSB.

10. Write short notes on ***any two*** : **2x5=10**

(a) Sample and Hold circuit.

(b) Cyclic DAC.

(c) High pass syncronous filters.