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BIELE-011

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00371 **December, 2017**

BIELE-011 : DIGITAL SYSTEM DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Use of scientific calculator is allowed.*

1. Expand the following function (f) to minterms and maxterms. Implement the function (f) using NAND gates only. *10*

$$f = (A + \bar{B})(CD + \bar{E})$$

2. Draw and explain the function of a 4-bit ring counter with its sequence table and state diagram. *10*

3. Design a 128 × 1 multiplexer by using 4 × 1 MUX only. How many numbers of 8 × 1 MUX are required to have a 256 × 1 MUX ? *10*

4. Design and implement an asynchronous 4-bit down counter using JK flip-flops. Draw the excitation table and corresponding state diagram also. *10*

5. Write a VHDL procedure ADDREC, which will add two N-bit vectors and a carry and returns an N-bit sum and a carry. The procedure call is of the form

ADDREC(A, B, Cin, Sum, Cout, N). *10*

6. Explain the different types of fault models and fault types in a PLA. Plot the following PLA on the map. Identify the undetectable faults. *10*

x_1	x_2	x_3	x_4	z_1	z_2
0	2	2	1	1	0
2	1	1	2	1	1
0	1	2	1	0	1

7. What is a ROM ? Draw the ROM cell and explain its operation. *10*

8. Design a Finite State Machine (FSM) that counts the following decimal sequence :

3, 7, 2, 6, 3, 7, 2, 6, ...

The count is to be represented directly by the contents of the D flip-flops. The counting starts when the control input C is asserted and stops whenever C is deasserted. Assume that the next state from all unused states is the state for the first count in the sequence. *10*

9. Design a 2-bit up counter using D flip-flops and implement it using suitable PAL. *10*