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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00331

Term-End Examination

December, 2017

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

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1. (a) Enlist VHDL capabilities as a language. *5*

(b) Write down different types of design units used in VHDL. *5*

2. (a) Define different styles of modelling used in VHDL. *5*

(b) Write the VHDL code for a full adder circuit using logic equations. *5*

3. (a) Why are configurations needed ? Explain with examples. *5*

(b) What is Subprogram Overloading ? What are its types ? *5*

4. (a) Write the syntax for package declaration and package body. *5*

(b) Write down the VHDL structural model code for D flip-flop. *5*

5. (a) Enlist the purpose of digital system testing. *5*

(b) Describe in brief, the various faults associated with digital circuits. *5*

6. Draw a flow chart of Automatic Test Pattern Generation (ATPG) for fault coverage. *10*

7. Give an example of a logic circuit in which stock-at-1 fault and stock-at-0 fault are indistinguishable. *10*

8. Define scan-based techniques with the help of a diagram. Also enlist various steps used for testing a sequence. *10*

9. What is Built-In Self-Test (BIST) technique ? Give essential circuit modules required for BIST. Explain any one of them. *10*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) Delay Models

(b) Ad-hoc Design for Testability Techniques

(c) FPGA