BIEE-017

B.Tech. – VIEP – ELECTRICAL ENGINEERING (BTELVI)

□□392   **Term-End Examination**

December, 2017

BIEE-017 : DIGITAL ELECTRONICS

Time : 3 hours   *Maximum Marks : 70*

*Note : Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

1. Simplify the following Boolean expressions to a minimum number of literals using laws of Boolean algebra :   *5×2=10*

    (a) $(x + y)(x + \bar{y})$

    (b) $xyz + \bar{x}y + xy\bar{z}$

    (c) $xz + \bar{x}yz$

    (d) $xy + x(wz + w\bar{z})$

    (e) $\bar{a}bc + ab\bar{c} + abc + \bar{a}b\bar{c}$

2. Find the complement of F = wx + yz and also prove that

    (a) $F \cdot \overline{F} = 0$,

    (b) $F + \overline{F} = 1$.   *2+4+4=10*

3. For the given Boolean function :

$F = \overline{x}\ \overline{z} + \overline{y}\ \overline{z} + y\overline{z} + xy$, determine

    (a)   the function F as a product of maxterms,

    (b)   Minimal POS expression,

    (c)   F as a sum of minterms.   *3+3+4=10*

4. What is a Full Adder ? Give its truth table. From its truth table, obtain the expression for sum and carry. Also implement a full adder using 2 half adders and an OR gate.   *2+2+2+4=10*

5. (a)   Implement a 4 × 16 decoder with the help of 3 × 8 decoders.   *5*

    (b)   Implement the Boolean function
        $F(x, y, z) = \Sigma (1, 2, 6, 7)$ using 4 × 1 MUX.   *5*

6. How can a T flip-flop be obtained using

    (a)   JK flip-flop ?

    (b)   D flip-flop ?   *5+5=10*

7. Explain with the help of a pin diagram, the architecture of 8085 CPU. *10*

8. Explain the various addressing modes of 8086. *10*

9. Explain the procedure for synthesis of a 3-bit counter using T flip-flop. Support your answer with the state table and logic diagram. *10*

10. Write short notes on any *two* of the following : *2×5=10*

   (a) Assembler Instruction Format

   (b) String and Stack Manipulation

   (c) Comparison of 8088 with 8086

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