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BIEL-012

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00679

Term-End Examination

December, 2017

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed. Use of scientific calculator is permitted.*

1. Define the terms Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs). Differentiate between analog and discrete-time signals. State the Nyquist criterion. *3+4+3=10*

2. Give the mixed-signal layout strategy indicating the steps from system level to interconnect level. Also give an example of a mixed-signal floor plan. *5+5=10*

3. What are the various techniques used to map the digital value into an analog quantity ? What are the different digital input codes ? Which is most frequently used and why ? Give their merits and demerits. *3+3+2+2=10*

4. Give the circuit diagram of a charge scaling DAC and prove that the output voltage is given as

$$V_{out} = \sum_{k=0}^{N-1} D_k 2^{k-N} V_{REF}.$$ *4+6=10*

5. What is a Comparator Circuit ? Give the schematic symbol and briefly explain its basic operation. Also draw the block diagram of a high performance comparator. *3+3+4=10*

6. Give the circuit diagram of a CMOS multiplier employing multiplying quad. Explain its operation and give the expression for its output voltage. *4+6=10*

7. Explain the use of decimating filters used for improving the signal-to-noise ratio (SNR) of ADCs. *10*

8. Draw the block diagram of a two-stage CMOS op-amp employing output buffer and explain the operation of each block. *10*

9. Explain the operation of MOSFET as a switch with necessary mathematical model and calculations. *10*

10. Write short notes on any ***two*** of the following : *2×5=10*

    (a) Delay Elements

    (b) Adder Elements

    (c) Resistor String DAC
