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BICS-022

B.Tech. – VIEP – COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

Term-End Examination

00257

December, 2017

BICS-022 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. Explain the following terms in the context of computer architecture : *10*

   (a) Mean Time To Failure and Mean Time Between Failures

   (b) Performance, execution time and their relationship

   (c) Benchmarks

   (d) Principle of Locality

   (e) CPU time and its relation to clock rate

2. What is Instruction Set Architecture (ISA) ? Explain the following terms in the context of an ISA : *10*

   (a) General purpose registers

   (b) Memory addressing

   (c) Addressing modes

   (d) Types and sizes of operands

   (e) Operations

   (f) Control flow instructions

3. (a) Consider the following program segment :

```
for (i = 0; i < 1000; i++)
  {
     a[i] = b[i] + c[i];
  }
```

   where a, b, c are arrays of size 1000. What kind of parallelism can be used to execute the program segment given above ? Give justification in support of your answer. *5*

   (b) What is data dependency in the context of instruction level parallelism ? Explain with the help of example. *5*

4. (a) How is instruction level parallelism handled using VLIW architecture ? Name one processor architecture that uses VLIW. *5*

   (b) Explain the levels of memory hierarchy in a desktop computer. Also explain the concept of n-way set associative cache placement mechanism. *5*

5. (a) Explain the following cache optimisation techniques with the help of an example each : 6

(i) Way prediction to reduce hit time

(ii) Merging write buffer to reduce miss penalty

(iii) Code and data rearrangement by compiler to reduce miss rate.

(b) List the basic problems relating to memory in a multicore processor based system. 4

6. (a) Explain the cache coherence in the context of a multiprocessor system with the help of an example. 5

(b) Explain the directory based protocol to maintain cache coherence in a shared memory based multiprocessor system. 5

7. (a) What is a symmetric shared memory architecture of a multiprocessor system ? List the advantages and disadvantages of using such architectures. 5

(b) What is Thread Level Parallelism ? How is it different to instruction level parallelism ? Can thread level parallelism be converted to instruction level parallelism ? Explain. 5

8. (a) Explain the meaning of model of memory consistency in the context of multiple processors. What is Sequential Consistency in this context ? 5

(b) Consider the following set of instructions :

```
ADD     R1, R2, R3   ;  R1 ← R2+ R3
BNZ     R1, LABEL1 ;  Branch to Label 1
                      if R1 is zero
BNC     LABEL2       ;  else branch to Label 2.
LABEL1 : ...
         .
         .
         .
LABEL2 : ...
         .
         .
         .
```

What kind of data dependencies exist in the above code ? Explain. *5*

9. (a) Differentiate between Single Instruction Stream, Single Data Stream (SISD) and Single Instruction Stream, Multiple Data Streams (SIMD) architectures. *5*

(b) Explain the process of floating point addition. How is the floating point addition operation performed in MIPS using pipelining ? *5*

10. Explain any ***four*** of the following with the help of a diagram/example, if needed : *10*

(a) Branch Prediction
(b) Virtual Memory
(c) DRAM
(d) Throughput in the Context of Computer Architecture
(e) Concept of Pipelining
(f) Interconnection Network