No. of Printed Pages : 3

BICS-009

B.Tech. – VIEP – COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

00527

Term-End Examination

December, 2017

BICS-009 : LOGIC DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. (a) Design a 2 input XOR gate of using number of NAND gates. 5

(b) Explain Positive logic and Negative logic. 5

2. (a) State and prove De Morgan's theorems. 5

(b) Obtain the canonical sum of product form of the following : 5

(i) $f = \bar{A}BC + \overline{B\bar{C}}(A + D)$

(ii) $f = A(C + \bar{D}) + B\bar{C}$

3. (a) What is a Decoder ? Draw neat diagrams for it. 5

(b) Write a short note on seven segment decoder. 5

4. (a) What is Even parity or Odd parity ? Explain parity checker and parity generation with the help of an example. 5

(b) With a neat sketch, explain Diode ROM. 5

5. (a) Add the following 8-bit numbers : 0101 0111 and 0011 0101, then show the same number in hexadecimal notation. 3

(b) Show the binary subtraction of 125_{10} from 200_{10}. 4

(c) Express 19750 in 2's complement representation. 3

6. (a) What is JK Flip-Flop ? Show in diagrams and write the truth table. 5

(b) How does the Schmitt trigger inverter work ? Explain. 5

7. (a) What are the types of Registers ? Explain with the help of neat diagrams. 5

(b) How does the 4-bit serial input shift register work ? Explain with the help of neat diagram. 5

8. (a) Show a method for constructing a 5×2 mod 10 decode counter. 5

(b) What is a Digital Clock ? Explain with the help of neat diagram. 5

9. (a) Find the output voltage from a 5-bit ladder that has a digital input of 11010. Assume that 0 = 0 V and 1 = + 10 V. *5*

(b) Find the binary equivalent weight of each bit in a 4-bit system in variable register network. *5*

10. What is a successive approximation converter ? Explain with the help of diagrams. *10*