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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00513

Term-End Examination

December, 2016

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed. Use of scientific calculator is permitted.*

1. Explain data flow style and mixed style of modelling with the help of suitable examples. *10*

2. (a) Differentiate between Scalar and Integer data type with suitable examples. *5*

   (b) Write a complete structural model for a 3-bit parity generator. *5*

3. (a) Differentiate between concurrent and sequential signal assignment with suitable examples. 5

(b) Define Generics. Write an entity for an AND gate which has nine generics. 5

4. (a) Explain Inertial and Transport delay models. 5

(b) Write the entity for routing delay model. 5

5. What is VHDL ? Explain the historic view and capabilities of this language in detail. 10

6. (a) What are the advantages of behavioural fault modelling ? 5

(b) Derive a test set for a two-to-one multiplexer for the functional fault model. 5

7. (a) Explain the term fault modelling. Also name the different types of fault models. 5

(b) Differentiate between structural and functional fault models. 5

8. (a) Derive the four-valued truth table of fault-free versions of each of the following : 5

(i) A two-input AND gate

(ii) A two-input NOR gate

(b) Explain the structure of n-stage Linear Feedback Shift Register (LFSR). 5

9. (a) Explain Random testing. Also derive the escape probability of fault. 5

(b) Explain the test points to improve testability. 5

10. (a) How will creating an internal line of circuit, through an observation point, improve the random pattern testability of the circuit ? 5

(b) Explain the architecture of field programmable gate array by taking a suitable example. 5