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BIELE-002

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00033

December, 2016

BIELE-002 : MICROELECTRONICS TECHNOLOGY

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Assume suitable missing data, if any. Use of scientific calculator is permitted.*

1. With a neat sketch, explain Czochralski (CZ) method of crystal growth in detail. *10*

2. Explain vapour phase epitaxy for silicon. Also discuss impurity redistribution during growth. *10*

3. Discuss the steps involved in CMOS-Inverter fabrication with suitable diagrams. *10*

4. Why is plasma etching preferred in CMOS IC fabrication ? Compare five different types of plasma etching systems. *10*

5. (a) What is lithography ? Explain with diagrams, the steps involved in photolithography. 5

(b) What is photoresist ? Give its classification with some examples. 5

6. Explain the growth mechanism and kinetics of oxidation using Deal-Grove Model. 10

7. (a) Explain the problems associated with silicon diffusion. 5

(b) Explain the range theory of ion-implantation. 5

8. Draw the sketches illustrating a (100) plane, a (110) plane and a (111) plane in a cubic unit cell. How many equivalent (100) planes are there in a cubic crystal ? A material has a face centred cubic structure with an ionic radius of 1·06 Å. Calculate the interplanar separation for (111) planes. 10

9. Write short notes on any ***two*** of the following : 2×5=10

(a) Interstitial Diffusion

(b) Oxide Isolation

(c) Dry and Wet Oxidation

10. (a) What are the films used for interconnection in single metal, multi metal, and multi level metallization schemes ? *3*

(b) Discuss the steps involved in integration of Bipolar process. *7*