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BIEL-025

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00423 **Term-End Examination**

December, 2016

BIEL-025 : ADVANCED MICROPROCESSOR ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Use of scientific calculator is allowed.*

1. (a) Define Bus and System Bus. What are the different types of System Bus ? *5*

(b) A digital computer system has a common bus system for 16 numbers of registers each of 32 bits. The bus is designed using multiplexers and decoder.

(i) How many select inputs are needed for MUX ?

(ii) How many decoders are required and what is their size ? *5*

2. Describe the instruction format and give examples of no-operand, one-operand, two-operand and three-operand instructions. *10*

3. Explain the causes of pipeline hazards and their remedy. *10*

4. Define Parallel Computing. What are the important features of parallel processing ? *10*

5. An 8-bit computer has a 16-bit address bus. The first 15 lines are used to select a word in bank of 04 k bytes of memory. The high-order bit of the address is used to select a register which receives the content of data bus. Explain how this configuration can be used to extend the memory capacity of the system to eight banks of 04 k bytes each. Draw the logic diagram also. *10*

6. (a) Discuss the difference between tightly coupled multiprocessor and loosely coupled multiprocessor from the viewpoint of hardware organization and programming techniques. *5*

   (b) Write the differences between centralised shared memory architecture and distributed shared memory architecture. *5*

7. With the help of pipeline diagrams, explain superscalar and VLIW processors. *10*

8. What is a compiler ? Explain the working details of a compiler. *10*

9. Interface an 8-bit microprocessor with a 2 k × 8 ROM chip and two numbers of 1 k × 8 RAM chip such that the following address map is realised :

Device	*Size*	*Address Assigned*
ROM Chip	2 k × 8	0000 – 07FF
RAM Chip-1	1 k × 8	0800 – 0BFF
RAM Chip-2	1 k × 8	1000 – 13FF

Draw the connection diagram and explain. *10*

10. (a) Distinguish between hardwired control units and microprogrammed control units. *5*

(b) Define Reducing Hit Time. Also discuss the issues in the design of Memory Hierarchy. *5*