BIEL-012

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)
Term-End Examination
December, 2016

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BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours   *Maximum Marks : 70*

*Note : Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed. Use of scientific calculator is permitted.*

1. (a) Explain the characteristics and typical errors associated with sample and hold circuit.   5

   (b) Discuss the advantages and disadvantages of using a dual slope over a single slope ADC.   5

2. (a) Explain qualitatively the architecture and working of charge scaling DAC.   5

   (b) Design a 3-bit charge scaling DAC and find the value of output voltage for $D_2D_1D_0 = 100$ and 011. Assume $V_{ref} = 5$ V, $C = 0.5$ PF.   5

3. (a) Briefly explain the architecture and working of pipeline digital-to-analog converter (DAC). 5

(b) Find the resolution of DAC, if the output voltage is desired to change in 1 mV increments while using a reference voltage of 4 V. 5

4. (a) Draw and explain the block diagram of a 2-step flash ADC. 5

(b) Explain Successive Approximation ADC with its block diagram. Also write down its advantages over pipeline ADC. 5

5. Explain qualitatively preamplification and decision circuits of a CMOS comparator unit. Draw its CMOS circuits. 10

6. (a) Describe the use of level shifting circuits in non-linear analog devices. 5

(b) Briefly explain CMOS analog multiplier with the help of a circuit diagram. 5

7. (a) Explain how SNR can be improved using signal averaging. 5

(b) Briefly explain the role of decimating filters in ADCs. 5

8. With a neat process flow diagram, explain submicron CMOS technology and bring out the differences as compared to CMOS technology. *10*

9. What are delay elements ? Explain how they are realized using pass transistors, inverters and C^2MOS and TSPC circuits. *10*

10. Write short notes on any *two* of the following : *2×5=10*

    (a) Op-Amp Design

    (b) High Pass Synchronous Filters

    (c) Mixed-Signal Layout Issues

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