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BIELE-015

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00175

Term-End Examination

December, 2014

BIELE-015 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Any missing data may be suitably assumed.*

1. Design a BCD adder by using logic gates and explain its operation. *10*

2. Describe IEEE 754 standard for floating point numbers. Explain the terms mantissa, exponent, base, guard bits and bias. *10*

3. (a) Draw and explain the architecture of an accumulator based CPU. *5*

(b) Explain data pipelining process for addition and subtraction of floating point numbers. *5*

4. Draw a space time diagram for a six-segment pipelining, showing the time it takes to process eight tasks. A non-pipeline system takes 50 ns to process a task. The same task can be produced in a six segment pipeline with a clock cycle of 10 ns. Determine the speed-up ratio of the pipeline for 100 tasks. What is the maximum speed-up that can be achieved ? *10*

5. (a) Give the circuit of data path for sequential n-bit binary divider. *5*

   (b) Explain the difference between hardwired control and microprogrammed control unit. Is it possible to have a hardwired control unit associated with a control memory ? *5*

6. (a) What is cache memory ? How is it implemented ? *5*

   (b) Describe the main advantages and disadvantages of memory segmentation. *5*

7. (a) What are the various mapping techniques used in the cache organisation ? Explain any one of them briefly. *5*

   (b) Draw the logic circuit for 1-bit associative memory cell and give its description. *5*

8. (a) What is the difference between intra and inter system communication methods ? *5*

(b) Explain why the single shared bus is so widely used as an interconnection medium in both sequential and parallel computers ? What are its main disadvantages ? *5*

9. Define each of the following I/O control methods : *10*

(i) Programmed I/O

(ii) Daisy chaining method

List the advantages and disadvantages of each method.

10. Write short notes on any ***two*** of the following : *2×5=10*

(i) Address space and Memory space

(ii) RAM and ROM chips

(iii) Superscalar processing