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BIELE-013

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00016

Term-End Examination

December, 2014

BIELE-013 : DEVICE MODELLING FOR CIRCUIT SIMULATION

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data may be suitably assumed. Calculators are permitted.*

1. Explain the effect of full-scaling and constant-voltage scaling on the operating characteristics of the MOS transistor. *5+5*

2. Give the simplest current-voltage relationship of n-channel MOSFET used for LEVEL-1 in SPICE for

(i) Linear Region

(ii) Saturation Region *5+5*

3. Explain the effect of base-narrowing in BJT's with suitable mathematical steps. *10*

4. Give the high frequency model of a diode and explain how we can measure the parameters of high-frequency model. *10*

5. Explain the method used in the extraction of MOSFET model parameters. *10*

6. Explain in brief the various channel mobility models of MOSFET. *10*

7. Explain the small-signal model of BJT. *10*

8. What do you understand by SPICE and how will you do the DC Analysis of a given circuit ? *10*

9. Discuss the principle of Heterojunction devices with suitable examples. *10*

10. Write short notes on any ***two*** of the following : *5+5*

    (i) MESFET

    (ii) JFET

    (iii) Drain Induced Barrier Lowering (DIBL)