No. of Printed Pages : 3

BIELE-011

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00915

Term-End Examination

December, 2014

BIELE-011 : DIGITAL SYSTEM DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. All questions carry equal marks.*

1. Design a sequential circuit with JK flip-flops to satisfy the following state equations : *10*

$$A(t + 1) = A'B'CD + A'B'C + ACD + AC'D'$$

$$B(t + 1) = A'C + CD' + A'BC'$$

$$C(t + 1) = B$$

$$D(t + 1) = D'$$

2. (a) What is the difference between ROM and PROM ? Give the applications of ROM and PROM. *5*

(b) What is the difference between PAL and PLA programming structure ? *5*

3. (a) Discuss the different types of faults in a digital circuit. *5*

(b) With an example, explain the principle of operation of path sensitisation method. *5*

4. (a) What is the difference between 'Mealy' and 'Moore' models of sequential machine ? Explain using structural diagram. *5*

(b) A combination circuit is defined by the following functions :

$$F_1(A, B, C) = \Sigma (3, 5, 6, 7)$$

$$F_2(A, B, C) = \Sigma (0, 2, 4, 7)$$

Implement the ckt with a PLA having three inputs, four product terms and two outputs. *5*

5. (a) Write an application of MC 2900 in system control design. *5*

(b) Discuss the concept and features of programmable system controller. *5*

6. Using MSI decoder, design MST circuits. *10*

7. Write the VHDL code for a full subtractor using *10*

(a) Behavioural Modelling

(b) Structural Modelling

8. Draw a block diagram for binary multiplier. Write a behavioural model for 4 × 4 binary multiplier. *10*

9. Write short notes on any ***two*** of the following : *2×5=10*

(a) Races, Cycles and Hazards

(b) Design of testability

(c) Field programmable logic arrays