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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00626

December, 2014

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data (if any) may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

1. Explain the importance of Hardware Description Language (HDL) in the design of digital systems. List some of the significant features. *10*

2. Define the terms — data objects and data types. Also give a comparison between the two. *4+6=10*

3. What do you understand by the term "Behavioural Modelling" ? How can it be used for the design of digital systems ? Give an example. *3+4+3=10*

4. What are the various advanced features available in VHDL ? Explain them. *4+6=10*

5. Differentiate between single and multiple stuck faults with the help of a suitable example. *10*

6. Give an algorithm for random test generation method used in testing single stuck fault. Give an example. *10*

7. What are the various testability techniques for the ad-hoc design of digital systems ? Give a simple example for each technique. *10*

8. With the help of an example, list the differences between VHDL simulator and VHDL synthesizer ? *10*

9. Write a program in VHDL for the following : *5+5=10*

   (a) Full-Adder

   (b) 8 : 1 Multiplexer

10. Write short notes on any ***two*** of the following : *5+5=10*

    (a) Built-In-Self-Test Architecture

    (b) Fault Models

    (c) Testing for bridging faults
