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BIELE-002

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00356

December, 2014

BIELE-002 : MICROELECTRONICS TECHNOLOGY

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. Assume suitable missing data, if any. Use of scientific calculator is permitted.*

1. (a) Describe the process of preparation of EGS from MGS.

   (b) Explain crystal orientations and orientation dependent properties of silicon crystals with suitable diagrams. *5+5=10*

2. (a) What is oxidation and what is its use in IC Technology ?

   (b) Explain the Deal-Grove model of describing kinetics of silicon oxidation. *3+7=10*

3. A process engineer building an NMOS device wants to dope the polysilicon at the same time as doing the Arsenic source/Drain diffusion. The source/drain implant dose is 2×10^{15} cm^{-2} at an energy of 50 eV.

(a) For the above implant conditions, what is the minimum polysilicon thickness that can be used if the implant is not to affect the channel doping which is 10^{16} cm^{-3} near the surface (Assume the gate oxide is of negligible thickness compared to the polysilicon) ?

[R_p = 35 nm and ΔR_p = 15 nm]

(b) Assuming that the polysilicon thickness is actually used, how much of the implant dose will penetrate the polysilicon mask if the process engineer decides to change the implant energy to 80 keV ?

[R_p = 55 nm and ΔR_p = 22·5 nm] *5+5=10*

4. (a) What is Lithography ? Discuss the complete basic steps involved in the lithographic process.

(b) What is photo resist and what is its use in lithographic process ? *5+5=10*

5. (a) What is the need of etching in IC fabrication technology ?

(b) What are the major differences between reactive ion etching and parallel-plate plasma etching ? Compare the advantages and limitations of these techniques. *2+8=10*

6. (a) Explain the diffusion process using Fick's one-dimensional diffusion equations.

   (b) How are diffusion constant and mobility of a semiconductor related ? *8+2=10*

7. Briefly describe the following steps in CMOS process flow : *4+3+3=10*

   (a) Process option for device isolation – shallow trench isolation

   (b) Gate formation

   (c) Contact and local interconnect formation

8. (a) What is annealing ? What is its use in IC fabrication technology ?

   (b) Explain the basic process of ion implantation by using basic layout. *3+7=10*

9. (a) Why is multilevel metallization required in modern fabrication techniques ?

   (b) What are the desired properties of the metallization for ICs ? *5+5=10*

10. Write short notes on any ***two*** of the following : *5+5=10*

    (a) Physical Vapour Deposition (VPE)

    (b) Molecular Beam Epitaxy (MBE)

    (c) Reactive Ion-Beam Etching (RIBE)