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BIEL-012

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING

(BTECVI)

Term-End Examination

December, 2014

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. Assume suitable missing data, if any. Use of scientific calculator is permitted.*

1. (a) Explain the operation of Sample-and-Hold Circuit.

(b) Find the maximum sampling error for a S/H circuit that is sampling a sinusoidal input signal that could be described as

$V_{in} = A \sin 2\pi ft$, where

$A = 2$ V and $f = 100$ kHz

Assume that the aperture uncertainty is equal to 0·5 ns. Also find the maximum resolution of an ADC which can use the above S/H circuit while maintaining a sampling error less than 1/2 LSB.

2×5=10

2. (a) What are the specifications of DAC and ADC ? Describe each.

(b) Find the resolution of a DAC, if the output voltage is desired to change in 1 mV increments while using a reference voltage of 5 V. *2×5=10*

3. What are the mixed-signal layout issues ? Explain using suitable diagrams. *10*

4. (a) What are the various DAC architectures that exist ? Explain pipeline architecture of DAC.

(b) Describe the Flash ADC architecture using suitable block diagram. *2×5=10*

5. Derive the expressions for the transconductance (g_m) and output resistance (r_o) of a MOSFET in the triode region. Plot these quantities and $g_m r_o$ as a function of V_{DS}, covering both triode and saturation regions. *10*

6. (a) What are the Op-amp design parameters ? Explain each.

(b) The circuit as shown in Figure 1 is designed for a nominal gain of 10. Determine the minimum value of A_1 for a gain error of 1%.

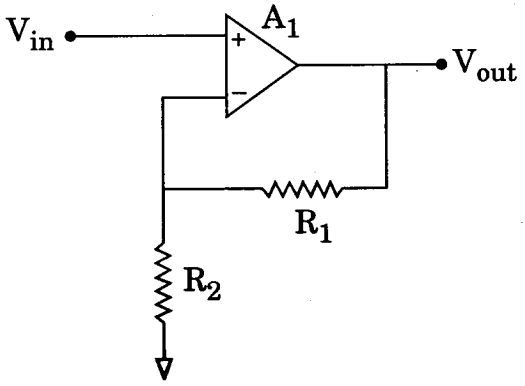

Figure 1

2×5=10

7. (a) What is sub-micron CMOS technology ? How is it different from CMOS technology ? Draw the process flow diagram of passive devices in sub-micron CMOS technology. *8*

(b) Explain the sub-micron CMOS issues during scaling. *2*

8. (a) How is SNR improved in data converters ? Explain.

(b) Differentiate between decimating filters for ADC and interpolating filters for DAC. *2×5=10*

9. What are the building blocks of a comparator ? Design a basic comparator using CMOS circuits. Explain its operation principle. *10*

10. Write short notes on any ***two*** of the following :

2×5=10

(a) Successive Approximation ADC

(b) Analog Multiplier

(c) Current Steering DAC