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MINI-034

M.Tech. IN ADVANCED INFORMATION TECHNOLOGY – MICROELECTRONICS AND VLSI DESIGN (MTECHVD)

Term-End Examination

00234

December, 2014

MINI-034 : SEMICONDUCTOR TECHNOLOGY

Time : 3 hours *Maximum Marks : 100*

Note :

(i) *Section I is **compulsory**.*

(ii) *In Section II, answer any **five** questions.*

(iii) *Assume suitable data wherever required.*

(iv) *Draw suitable sketches wherever required.*

SECTION I

1. Suppose that you are required to specify the resist thickness that will be used in a production lithographic process. The following data are available :

(a) 1·5 μm minimum feature must be printed. Resolution is adequate when the resist thickness T is in range 0·5 to 2·0 μm, but feature size control is better for thinner resists.

(b) Each wafer has 150 chip sites; each chip has a 0.1 cm^2 active area.

(c) Five mask levels are required to complete device.

(d) 2000 finished wafers must be produced each day (20 hr per day = 3 shifts).

(e) The resist defect density D_0 increases as the resist is made thinner, where D_0 is the number of defects per square centimeter, and is approximated by $D_0 = 1 \cdot 4\ T^{-3}$. T is in microns.

(f) The chip yield (percentage good) can be approximated at each mask level by $y = (1 + qD_0a)^{-1}$, where q is the fraction of defects that render a chip inoperable (fatality rate) and 'a' is the active area of chip.

(g) On an average, 50% of the defects are fatal defects.

(h) More time is needed to expose thick resist than to expose thin resist. The exposure tool throughput in wafers/hr is approximated by $125 - 50T$ for $(0 \cdot 5 \le T \le 2 \cdot 0\ \mu m)$.

Answer the following questions :

(i) Specify the resist thickness to be used and justify your recommendation.

(ii) If exposure tools cost ₹ 350,000 each, what is the difference in equipment cost for a process using 1 μm and 1·5 μm of resist ? *15+15=30*

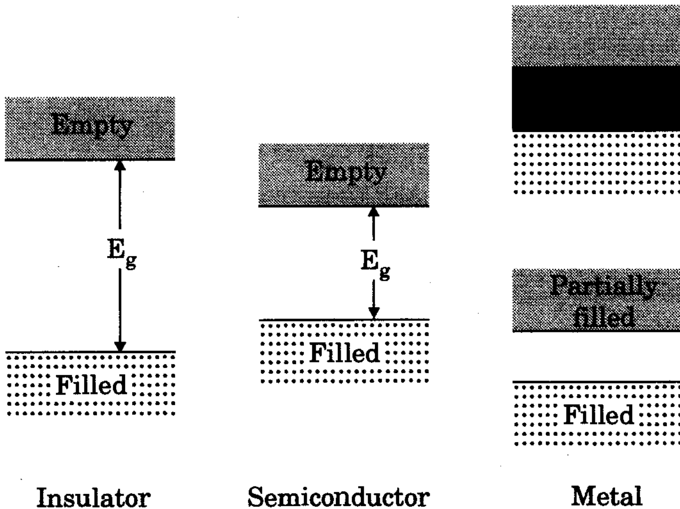
SECTION II

2. An Si crystal is to be grown by the Czochralski method, and it is desired that the ingot contain 10^{16} phosphorus atoms/cm^3.

(a) What concentration of Arsenic atoms should the melt contain to give this impurity concentration in the crystal during the initial growth ? For As in Si, $k_d = 0{\cdot}3$. (Note : Assume that $C_s = k_d C_L$ throughout the growth.)

(b) If the initial load of Si in the crucible is 5 kg, how many grams of phosphorus should be added ? The atomic weight of phosphorus is 31. (Note : Density of Si is 2·33 g/cm^3) *7+7=14*

3. "Semiconductor materials at 0 K have basically the same structure as insulators." Prove this statement, whether correct or not, with the help of Typical band structures at 0 K shown in figure below. *14*



4. What is homo and hetero epitaxy ? What is the purpose of homo epitaxy ? Give suitable example. *4+5+5=14*

5. In the fabrication laboratory of CISR, Indian scientists want to fabricate Integrated Chips of the basic microprocessor. Explain which basic steps for the fabrication must be followed by the scientists and why. *14*

6. While fabricating VLSI chip, which oxidation-induced defects can get added ? List the possible ways of growing an oxide on a substrate without forming oxidation-induced stacking faults. *7+7=14*

7. High-temperature stability of metal films on lightly doped silicon can be investigated by measuring the resistivity changes of the metal film as a function of annealing temperature. Design the experiment and state the assumptions you need to make for this study. *14*

8. What are the major distinctions between reactive ion etching and parallel plate plasma etching ? Compare the advantages and limitations of this technique. *7+7=14*