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**MINE-052**

# M.Tech. IN ADVANCED INFORMATION TECHNOLOGY - EMBEDDED SYSTEM DESIGN (MTECHSD)

## Term-End Examination

## December, 2014

00270

## MINE-052 : FPGA BASED EMBEDDED SYSTEM DESIGN

*Time : 3 hours* *Maximum Marks : 100*

***Note :***

*(i)* *Section I is* ***compulsory****.*

*(ii)* *In Section II, answer any* ***five*** *questions.*

*(iii)* *Assume suitable data wherever required.*

*(iv)* *Draw suitable sketches wherever required.*

*(v)* *HDL code signifies student can write code in any hardware description language i.e. VHDL or Verilog.*

*(vi)* *Use of scientific calculator is allowed.*

## SECTION I

1. A user wants to display four BCD Data value to four multiplexed 7 segment display. Design appropriate FPGA controller to perform the given operation. *30*

Note : Components interfaced with FPGA having following specifications:

(a) Common anode 7 segment display

(b) 7 segment select transistors used are BC547 (NPN)

## SECTION II

**2.** Design a universal 4-bit binary counter which has the following facilities :

(a) It should perform up and down counting according to input signal UP_DN; If UP_DN = '1' then up counting otherwise down counting. *7*

(b) If input load signal LOAD = '1' then it should load data from input 4-bit LOAD_DATA to counter. *7*

**3.** If a digital system is performing multiple multiply and accumulation operation simultaneously, then for this system, which of microcontroller or FPGA is suitable ? Why ? Write VHDL code of full adder using half adders in structural style. *14*

**4.** What is PLD ? Provide different types of PLDs available in the market currently. Draw the basic architecture of FPGA. What is the role of CLB in FPGA ? *14*

**5.** What is the use of decoder in memory ? Explain with a neat block diagram. Write VHDL code for 3:8 decoder. *14*

**6.** What is the significance of blocking and non-blocking assignments in Verilog ? Illustrate with proper example. *14*

7. Write steps for implementing system in FPGA using Xilinx ISE. What is synthesis process in the implementation of FPGA ? Explain with a suitable example. *14*

8. (a) What are the advantages of using VHDL in the design of digital circuits, systems for PLDs and digital ASICs ?

   (b) What is intellectual property (IP) ? What are the main differences between a soft-core and a hard-core intellectual property (IP) block ? For the main PLD vendors, identify the types of processors that they support as IP blocks and whether they are provided as soft core or hard core IPs. *7+7=14*