B.TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

December, 2013

BIELE-003 : MODELING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *(i)* *Attempt any **seven** questions.*

(ii) *Assume suitable data if **missing**.*

(iii) *All question carry **equal** marks.*

1. (a) What important descriptive features of HDLs is not common to conventional high-level programming language ? 5

   (b) Can every VHDL Program that can be simulated be synthesized ? If not, explain why ? 5

2. (a) Which of the following can be used as a valid identifier in a VHDL program and which cannot ? 5

   (i) Adder

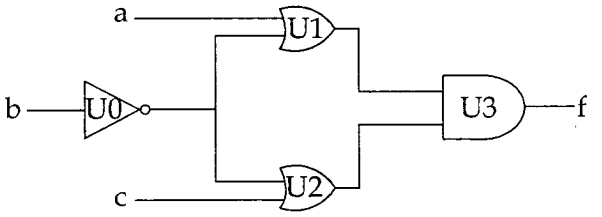
   (ii) 4 : 1 MUX

   (iii) TOP - LEVEL

   (iv) RESULT

(b) What is the difference in operation of a Port of mode IN,OUT and one of mode buffer ? Explain with suitable diagram. 5

3. For the logic diagram shown below : 10



Write a complete structural style design description consisting of a single design file. This description should correspond as closely as possible to the diagram. Use direct design entity instructions. Also, use named association in the port maps.

4. List and define the four classes of VHDL objects. Which of these classes are not common to conventional programming languages ? Which classes are synthesizable and which are not ? How are the classes that are not synthesizable used ?

2+2+2+4=10

5. Design an FSM that sets an output **z** to high when it detects a sequence of 0110 on the input **x**. Also draw the Mealy state diagram. 10

6. Differentiate the single stuck faults and multiple stuck faults with suitable diagram. 10

7. Explain the following test pattern generation methods : **5+5=10**

   (a) Weighted Test Generator

   (b) Adaptive Test Generator

8. What is Redundancy in testing ? Explain. Enlist undetectable fault in combinational circuit and also illustrate how they can be detect ? **3+7=10**

9. Explain the Ad-hoc design for testability techniques. **10**

10. Draw the FPGA architecture. Give the classification of FPGA and also explain CLB. **4+3+3=10**