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BIEL-030

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DIPLOMA VIEP ELECTRONICS AND COMMUNICATION ENGINEERING (DECVI)/ ADVANCED LEVEL CERTIFICATE COURSE IN ELECTRONICS AND COMMUNICATION ENGINEERING (ACECVI)

Term-End Examination

December, 2013

BIEL-030 : DIGITAL ELECTRONICS

Time : 2 hours *Maximum Marks : 70*

Note : *(i) Attempt **any five** questions. Each carry **equal** marks.*

*(ii) Question no. **one** is **compulsory** (objectives).*

*(iii) **All** the questions are to be answered in English Language **only**.*

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1. Attempt all objective questions : **2x7=14**

(a) Given binary number is 00000111, its 2's complement in Hexadecimal form is :

(i) F8 (ii) F9

(iii) O7 (iv) F3

(b) For a 4096×8 EPROM, the number of address lines is :

(i) 14 (ii) 10

(iii) 12 (iv) 16

(c) $A + A.B =$ _____.

(i) B (ii) AB

(iii) $A + B$ (iv) A

(d) A 4 bit binary number whose 2's complement is also same is _____.

(i) 0001 (ii) 0101

(iii) 1000 (iv) 0111

(e) In a Right Shift register, shifting a bit by one means :

(i) Multiplication by 2.

(ii) Division by 2.

(iii) Subtraction of 2.

(iv) Addition of 2.

(f) Which has the lowest propagation delay ?

(i) ECL (ii) TTL

(iii) PMOS (iv) CMOS

(g) A XNOR gate has inputs A and B and output Y. Then the output equation is

(i) $Y = \overline{A}B + A\overline{B}$ (ii) $Y = \overline{A}\,\overline{B} + AB$

(iii) $Y = AB + \overline{A}B$ (iv) $Y = A\overline{B} + AB$.

2. (a) Give the binary, BCD, excess-3, gray code, Hexadecimal and Octal representations of decimal numbers 6 and 9. **2x7=14**

(b) Design a gray to binary converter circuit of 3-bit (variable).

3. (a) Simplify the given Boolean Function using K-map and implement the minimized expression using Logic gates. **2x7=14**

$f(A, B, c, d) = \Sigma m(0, 1, 5, 9, 13, 14, 15) + d(3, 4, 7, 10, 11)$.

(b) Using NOR gate implement OR, AND, XOR and XNOR gates.

4. (a) Implement 16 : 1 multiplexer using 4 : 1 multiplexer. **2x7=14**

(b) Explain with truth table and waveforms a 4-bit Johnson Counter.

5. (a) Explain the operation of 4-bit PIPO (Parallel input parallel output) shift register with a neat diagram. **2x7=14**

(b) Realize 2-input NAND gate using TTL Logic and explain its operation.

6. (a) Draw the circuit diagram of JK Flip Flop with preset and clear inputs and explain its operation. **2x7=14**

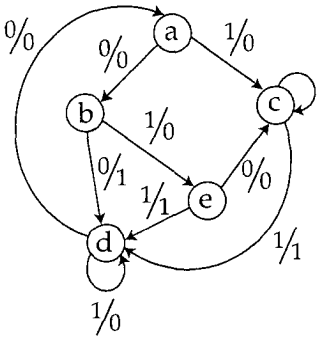
(b) Draw the truth table of Full adder and implement it with Half adders. Also derive the expression for sum and carry using K-Map.

7. (a) Convert the following functions to canonical form. **2x7=14**

(i) $Y = A + BC + ABC$.

(ii) $Y = (A + B)(\overline{B} + C)$.

(b) Obtain the reduced state table and reduced state diagram for a sequential circuit whose state diagram is shown in fig.



8. Write short notes on **any four** : **3.5x4=14**

(a) SRAM

(b) 2's complement subtraction.

(c) CMOS Logic Family.

(d) D/A converters.

(e) Moore Machine and Mealy Machine.

(f) Boolean algebra - Basic laws.