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BIELE-015

001181

B.TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

December, 2013

BIELE-015 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **any seven** questions. All questions carry **equal** marks. Any missing data may be suitably assumed and mentioned.*

1. (a) Explain the different cycles of an instruction. **3**

(b) What is CISC ? Explain its characteristics. **3**

(c) Discuss the advantages and disadvantages using a variable length instruction format. **4**

2. (a) Why is memory system of a computer organized as a hierarchy ? Discuss the basic elements of a memory hierarchy. **5**

(b) Define interrupt. When a device interrupt occurs how does the processor determine which device has issued the interrupt ? **5**

3. How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is; **5+5**

(a) a computational type requiring an operand from memory.

(b) a branch type.

4. List and define three techniques for performing I/O job. **10**

5. (a) Calculate average access time ($\bar{t}$), ratio of main memory time to cache memory time (y), and the value for efficiency of a system that contains cache memory (A) of a memory system whose performance are a indicated **7**

   Cache access time (t_c) = 160nsec.

   Main memory access time (t_m) = 960nsec.

   Hit ratio (h) = 0.90

   (b) What is the difference between a direct and an indirect address instruction ? How many references to memory are needed for each type of instruction to bring an operand into a processor register ? **3**

6. Draw and explain the block diagram of a typical DMA controller. **10**

7. (a) Explain the subcycles of instruction cycle with an example. **4**

   (b) Draw and explain hardwired control unit. Compare hardwired control unit and micro programmed control unit. **6**

8. (a) How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes ? **2**

   (b) How many lines of the address bus must be needed to access 2048 bytes of memory ? **4**

   (c) How many lines must be decoded for chip select ? Specify the size of decoder. **4**

9. Explain the concept and structure of Associative memory in detail with the help of neatly labelled block diagram. **10**

10. Assume a main memory has 4 page frames and initially all frames are empty. Consider the following stream of references, 1, 2, 3, 4, 5, 1, 2, 6, 1, 2, 3, 4, 5, 6, 5. **10**

Calculate the hit ratio if the replacement policy used are as follows :

(a) FIFO

(b) LRU