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BIEL-025

B.Tech. in Electronics and Communication Engineering (BTECVI)

Term-End Examination

December, 2013

BIEL-025 : ADVANCE MICROPROCESSOR AND ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *(i) Attempt **any seven** questions.*

*(ii) All questions carry **equal** marks.*

*(iii) Use of **Scientific** calculator is **allowed**.*

1. The output of four registers R_0,R_1,R_2 and R_3 are connected through 4-to-1 line multiplexers to the input of fifth register, R_5 . Each resister is eight bits long. The required are dictated by four timing variables to T_0 through T_3 as follows : **10**

T_0 : $R_5 \leftarrow R_0$

T_1 : $R_5 \leftarrow R_1$

T_2 : $R_5 \leftarrow R_2$

T_3 : $R_5 \leftarrow R_3$

The timing variables are mutually exclusive which means that only one variable is equal to 1 at any given time, while other three are equal to 0. Draw a block diagram showing the hardware implementations of register transfers, include the connections necessary from four timing variables to selection inputs of the multiplexers and to load input of register, R_5.

2. Write the difference between a microprocessor and a micro-program ? Is it possible to design a microprocessor with a micro-program ? Are all micro programmed computers also microprocessors ? 10

3. Why the theoretical treatment of parallolism is needed ? Explain Data and Resource Dependencies ? 10

4. Explain Instruction-Set Architecture. Also give characteristics of CISC and RISC Architecture. 10

5. Explain the structure and operational requirements of the instruction pipelines used in superscalar processors. Comment on the cycles per instruction expected from this architecture. 10

6. Explain the inclusion property and memory coherence requirements in a multi level memory hierarchy. Distinguish between write through and write back policies in maintaining the coherence in adjacent levels. 10

7. Explain the following terms associated with cache and memory architecture. 10

   (a) Low order memory interleaving.

   (b) Physical address cache versus virtual address cache.

   (c) Atomic versus non atomic memory access.

   (d) Memory bandwidth and fault tolerance.

8. Explain the concept of virtual memory. Also explain the virtual memory models. What are the memory replacement policies ? **10**

9. Consider the execution of a program of 15,000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out of sequence executions are ignored. **10**

   (a) Calculate the speed up factor in using this pipeline to execute the program as compared with the use of an equivalent non pipelined processor with an equal amount of flow through delay.

   (b) What are the efficiency and throughput of this pipelined processor ?

10. Consider the following reservation table for a four-stage pipeline with a clock cycle c = 20 ns. **10**

	1	2	3	4	5	6
S_1	X					X
S_2		X		X		
S_3			X			
S_4				X	X	

   (a) What are the forbidden latencies and the initial collision vector ?

   (b) Draw the state transition diagrams for scheduling one pipeline.

(c) Determine the MAL associated with the shortest greedy cycles. Determine the pipeline throughput corresponding to the MAL and given C. Determine the lower bound on the MaL for this pipeline. Have you obtain the optimal latency from the above state diagram ?
