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BICS-009

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B.TECH. COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

Term-End Examination

December, 2013

BICS-009 : LOGIC DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *(i) All questions carry **equal** marks.*

(ii) Assume suitable missing data if any.

*(iii) Attempt **any seven** questions.*

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1. (a) List non degenerate forms for two level implementations. Explain AND-OR-INVERT implementation. **5**

(b) Simplify the Boolean function : **5**
$F(w, x, y, z) = \Sigma(1, 3, 7, 11, 15)$
and don't cares:
$d(w, x, y, z) = \Sigma(0, 2, 5)$

2. What are the applications of Multiplexer ? Design 16 : 1 MUX using 4 : 1 MUX'S. **10**

3. (a) Differentiate in Encoder and Decoder. Design 4 input priority encoder. **5**

(b) Design 2 bit by 2 bit Binary Multiplier using Half adders and logic gates only. **5**

4. Implement and explain Master Slare JK flip-flop using clocked RS flip-flop. Also design Toggle and Delay flip-flop using Master Slare JK flip-flop. **10**

5. (a) Differentiate in shift register and counter. Explain 4 bit universal shift register using multiplexers. 5

(b) Define the term Modulus. How you can change the modulus of the counter ? 5

6. (a) Explain the differences among a truth table, a characteristic table, state table and an excitation table. 5

(b) Explain the methods to ensure a race free statement assignment. 5

7. (a) Design a 4 bit R-2R ladder type D/A converter and explain. 5

(b) Describe linearity, accuracy and resolution for D/A converter. 5

8. Draw the CMOS universal gate circuit and explain its complete operation. 10

9. Explain TTL - 3 input NAND gate operation using tristate logic and totem pole output stage with help of diagram. 10

10. Write short note on **any two** : 5x2=10

(a) Parity Generator and checker

(b) V-F converter

(c) TTL parameter and its open collector output configuration