BPHET-143

# ASSIGNMENT BOOKLET

**BACHELOR'S DEGREE PROGRAMME**
**(BSCG)**

## DIGITAL AND ANALOG CIRCUITS AND INSTRUMENTATION

**Valid from 1st January, 2025 to 31st December, 2025**

**School of Sciences**
**Indira Gandhi National Open University**
**Maidan Garhi, New Delhi-110068**
**(2025)**

Dear Student,

Please read the section on assignments in the Programme Guide for B.Sc. that we sent you after your enrolment. A weightage of 30 per cent, as you are aware, has been earmarked for continuous evaluation, **which would consist of one tutor-marked assignment** for this course. The assignment is in this booklet, and it consists of two parts: Part A and Part B. The total marks of both parts are 100, of which at least 35% are needed to pass.

**Instructions for Formatting Your Assignments**

Before attempting the assignment please read the following instructions carefully:

1) On top of the first page of your answer sheet, please write the details exactly in the following format:

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**ROLL NO.:** ……
**NAME:** ……
**ADDRESS:** ……
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**COURSE CODE:**……..
**COURSE TITLE:** ……
**ASSIGNMENT CODE:** ……..
**STUDY CENTRE:** …….. **DATE:** ……...

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**PLEASE FOLLOW THE ABOVE FORMAT STRICTLY TO FACILITATE EVALUATION AND TO AVOID DELAY.**

2) Use only foolscap size writing paper (but not of very thin variety) for writing your answers.

3) Leave 4 cm margin on the left, top and bottom of your answer sheet.

4) Your answers should be precise.

5) Solve Part A and Part B of this assignment, and **submit the complete assignment answer sheets containing Parts A and B within the due date.**

6) The assignment answer sheets are to be submitted to your Study Centre as per the schedule. **Answer sheets received after the due date shall not be accepted.**

   **We strongly suggest that you retain a copy of your answer sheets.**

7) This assignment is **valid from 1st January, 2025 to 31st December, 2025**. If you have failed in this assignment or fail to submit it by 31st December, 2025, then you need to get the assignment for the year 2026, and submit it as per the instructions given in the Programme Guide.

8) **You cannot fill the examination form for this course** until you have submitted this assignment. For any queries, please contact: sgokhale@ignou.ac.in. Please note that, we do not provide answers to Assignment questions.

We wish you good luck.

**Tutor Marked Assignment**

# DIGITAL AND ANALOG CIRCUITS AND INSTRUMENTATION

**Course Code: BPHET-143**
**Assignment Code: BPHET-143/TMA/2025**
**Max. Marks: 100**

**Note: Attempt all questions. The marks for each question are indicated against it.**

## PART A

1. a) Describe the formation of depletion layer in a *p-n* junction diode. Explain the *I-V* characteristics of *p-n* junction in forward and reversed biased conditions. (5)

   b) The intrinsic carrier concentration of a semiconductor is $3\times10^{17}\ m^{-3}$. It is doped with a trivalent impurity with dopant atom density of $8\times10^{18}\ m^{-3}$. The electron and hole mobilities are $0.5\ m^2\ V^{-1}s^{-1}$ and $0.3\ m^2\ V^{-1}s^{-1}$ respectively. Calculate its conductivity before and after the doping. (5)

2. a) Explain the working of *p*-channel JFET using a circuit diagram showing its voltage biasing with appropriate polarities. Draw its drain characteristics with $V_{DS} < 0$ V and $V_{GS} \geq 0$ V. (4+2)

   b) Discuss the breakdown mechanisms observed in a zener diode. (4)

   c) *h*-parameters of a single stage *CE* amplifier are given as $h_i$ = 2 kΩ , $h_r = 3 \times 10^{-4}$, $h_f$ = 85 and $h_o$ = 15 $\mu AV^{-1}$. Calculate $A_i$, $A_v$, $Z_{in}$ and $Z_{out}$ with $r_L$ = 10 kΩ and $r_S$ = 100 Ω. (5)

3. a) Convert $FC_{16}$ (Hex) into its binary equivalent and then divide it by $1001_2$. Express the result in octal equivalent. (5)

   b) Draw the circuit of 2-input NAND gate using diodes, transistor and resistors and explain its working with the help of truth table. (5)

4. a) Design a binary adder circuit to add 4-bit binary numbers corresponding to the decimal numbers 11 and 7. (5)

   b) Construct the Karnaugh map for the following 3-input truth table, write its Boolean expression and simplify it to obtain MSP. (3+1+1)

| *A* | *B* | *C* | *Y* |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

c) With the help of a suitable diagram, explain the subtraction of binary equivalent of decimal number 5 from binary equivalent of decimal number 7 using a 2's complement binary adder-subtractor. (5)

## PART B

5. a) Why is a Class *A* amplifier preferred over Class *C* amplifier in spite of being less efficient? (2)

b) Why is it necessary to use matched pair of transistors in a push-pull amplifier? (2)

c) An amplifier has maximum voltage gain of 500. Express it in dB scale. Calculate the gain at the cut-off frequencies on dB scale. (2+1)

d) What are the advantages of transformer coupling between the two stages of a cascade amplifier? (3)

6. a) State the Barkhausen criterion for sustained oscillations. Explain the operation of Colpitt Oscillator. For a Colpitt oscillator with 10 MHz frequency determine the equivalent capacitance, *C* forming tank circuit with 0.1 mH inductor. (6)

b) In a voltage regulator circuit, the output voltage under no load condition is 12V while under full load it is 11.8V. Over the full range of input voltage variation the nominal voltage output of 12V varies by 50 mV. Calculate percentage load and line regulation. (4)

c) Design and draw a circuit of series pass voltage regulator to provide 25 V output voltage and 160 mA maximum load current using a silicon *n-p-n* transistor with $\beta$ =80. Assume the input unregulated voltage to be 30 V and minimum zener diode current to be 10 mA. Specify the voltage and power rating of zener diode as well as value and power rating of the resistor used. (5)

7. a) Draw a circuit of a non-inverting amplifier with gain 1 using op-amp. Draw the output voltage curve of this circuit for a step input of 5V amplitude and 50 kHz frequency, if the slew rate of the op-amp is 0.5 V/$\mu$s. (Use proper scale on the time axis to illustrate the effect of slew rate). (5)

b) Design and draw the circuit of a three channel op-amp adder with channel gains of $-5$, $-10$ and $-15$ respectively. (5)

c) Explain the terms CMRR and input offset voltage in case of op-amp. (5)

8. a) State the main subsystems of a CRO and explain their functions. (5)

b) Design an astable multivibrator using IC 555 timer to generate a rectangular wave of 60% duty cycle at 10 kHz frequency. (5)

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