No. of Printed Pages : 3

BIEL-030

DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING (DECVI)

00024

Term-End Examination

June, 2011

BIEL-030 : Digital Electronics

Time : 2 hours *Maximum Marks : 70*

Note : *Attemt **any five** questions. Each carry **equal** marks. Question no **one** is **compulsory** (objectives). Give answer precisely and accurate.*

1. Attempt all objectives questions. **7x2=14**

(a) 1^s complement of the 101011 is

(i) 010100 (ii) 000000

(iii) 111111 (iv) 100000

(b) The expression $\overline{ABC}$ can be simplified

(i) $\overline{A}\,B\,\overline{C}$ (ii) $AB + BC + CA$

(iii) $AB + \overline{C}$ (iv) $\overline{A} + \overline{B} + \overline{C}$

(c) The Universal gates are

(i) NAND and NOR

(ii) AND and OR

(iii) OR and X-OR

(iv) None

(d) 3x8 Decoder have

(i) 3 I/p^s and 8 $0/p^s$

(ii) 8 I/p^s and 3 $0/p^s$

(iii) 8 I/p^s and 8 $0/p^s$

(iv) none

(e) The following is not a sequential circuit.

(i) J-K flip-flop

(ii) Counter circuit

(iii) Full adder

(iv) Shift Register

(f) MUX have

(i) many I/p^s and one O/p

(ii) one I/p^s and many O/p^s

(iii) one I/p^s and one O/p

(iv) None.

(g) Combinational circuits are designed with.

(i) feedback

(ii) without feedback

(iii) either (i) or (ii),

(iv) None.

2. (a) Converts the following base. **2x7=14**

(i) $(1010.11)_2 = (P.)_8 = (P.)_{16} = (P.)_{10}$

(ii) $(3AE5)_{16} = (P.)_8 = (P.)_{10} = (P.)_2$

(iii) Add $(3269)_{12} + (2368)_{12}$ without changing base

(b) Realize the following function using basic gates.

(i) $Y = AB\overline{C} + \overline{A}BC + ABC$

(ii) $Y = ABCD + \overline{A}BC\overline{D} + AB\overline{C}\,\overline{D}$

3. (a) Converts the following into canonical form. **2x7=14**

   (i) $AB + BC + CA$

   (ii) $(A+B).\ (B+C).\ (C+A)$

   (b) Minimize the following using K-MAP.

   (i) $f(w,x,y,z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$

   (ii) $F(A,B,C,D) = \sum \pi(2,3,4,5,6,7,11,14,15)$

4. (a) Design a gray to binary converter ckt of 3 bit (variable). **2x7=14**

   (b) Write the steps for combination ckt Design and design a full adder ckt with basic gates.

5. (a) Give difference between combinational ckt and sequential ckt and Design a S-R flip-flop Using NAND gates. **2x7=14**

   (b) Design a Asynchronous MOD 8 counter ckt.

6. (a) Design a 8×1 Multiplexer circuit and give the application of MUX. **2x7=14**

   (b) Design a 4 bit shift Register ckt.

7. Write the short notes on *any two*. **14**

   (a) Propagation delay and Fan In and Fan out

   (b) C MOS Inverter ckt.

   (c) TTL logic family.

   (d) EPROM and EEPROM.