B.TECH. IN COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

Term-End Examination

June, 2011

BICS-009: LOGIC DESIGN

Time: 3 hours Maximum Marks: 70

Note: Attempt any five questions. All questions carry equal marks.

- (a) Realize the Basic Logic gate using two input 5
 NAND Gate.
 - (b) Minimize the following function by 9

 Quine-McClusky method

$$f(A, B, C, D) = \sum_{m} (0.2,3,6,7,8,9,10,13)$$

2. (a) Using four-Input MUX, Implement the 7 following function:-

$$F(A, B, C) = \sum_{m} (0.2,3,5,7)$$

Control variable A and B

(b) Explain the operation of 4 I/P priority 7 Encoder.

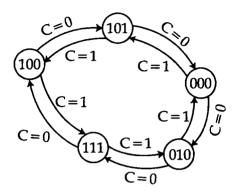
- 3. (a) Explain the method used for fast addition 7 and Draw its circuit.
 - (b) Draw and write the expression for a 4-bit parallel subtractor using full adder.
- 4. (a) Discuss the race around condition and 3+6 explain the operation of the circuit of its solution.
 - (b) Using TFF, Design RSFF. 5
- 5. (a) Explain the different modes of operation of a shift register with diagram.
 - (b) Implement MOD-8 Synchronous counter 7 with SR FFs.
- 6. (a) An asynchronous circuit is described by the following excitation and output function

$$Y = x_1x_2 + (x_1 + x_2) y ; Z = y$$

- (i) Draw the logic diagram and
- (ii) Derive the transition table, output map, flow table

(b) Implement the state Transition diagram shown in fig below using T FFs.

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- 7. (a) With neat diagram, explain R-2 R ladder 7 type D/A converter.
 - (b) Explain with neat diagram an open 7 collector TTL NAND gate.