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CS-12

03319

ADCA / MCA (III Year)

Term-End Examination

June, 2011

CS-12 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 75*

Note : ***Question** no. **1** is **compulsory.** Answer **any three** questions from the rest.*

1. (a) The SPARC architecture can be implemented with two to eight register windows for a total of 40 to 130 GPRs (general purpose registers) in the Integer Unit. Explain how the GPRs are organised into Overlapping Windows in each of the following designs : **10**

(i) Use 10 GPRs to construct two windows

(ii) Use 72 registers (GPRs) to construct four windows.

(iii) In which sense the SPARC is considered a scalable architecture ?

(iv) Explain how to use the overlapped windows for parameter passing between the calling procedure and the called procedure.

(b) Compare between multiprocessor and multi computer systems ? Also, explain various classification of multiprocessor systems. 7

(c) Explain the relationship between the integer unit and floating point unit in a RISC processor with scalar or super scalar organisations. 5

(d) Define multivector computing. Also, explain, how multivector computing is useful for super computers ? 5

(e) Compare between 'Private Cache' and 'Shared Cache'. 3

2. (a) Describe the importance of dynamic interconnection network characteristics in terms of minimum latency for unit data transfer, writing complexity, connectivity and routing complexity. 8

(b) What are the important characteristics of parallel algorithms which are machine implementable ? Also, explain suitability of parallel machines in implementation of these characteristics. 7

3. (a) Illustrate a diagram showing a synchronous bus timing using a four edge hand shaking (Inter locking) with variable length signals for different speed devices. 5

(b) What causes a processor pipeline to be under pipelined ? 5

(c) Compare and Contrast Central Arbitration with Distributed Arbitration. 5

4. (a) Make a data flow graph of the following expression evaluation : 5

$X = (a*c)/(b*a) - (d + c)$

(b) What makes the design of pipeline processors challenging ? What are exception conditions ? Briefly discuss the procedure to be followed when exceptions occur. What are other issues which complicate the problem ? 10

5. Write short notes on the following : 15

(a) Full Scale Vector Super Computers

(b) VLIW Architecture

(c) Hypercube inter connection Architecture

(d) SIMD

(e) MIMD