No. of Printed Pages : 3

BICS-009

B.TECH. IN COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

Term-End Examination

December, 2011

BICS-009 : LOGIC DESIGN

00762

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **any five** questions.*

1. (a) Realize the Basic logic gate using TWO inputs NOR gate. 5

   (b) Obtain a minimal pos form for the expression given below. 9
   $Y = \pi M(0, 1, 9, 10, 11, 13, 14, 15, 16, 17, 22, 23, 26, 27)$

2. (a) Design a BCD to seven segment decoder circuit. 7

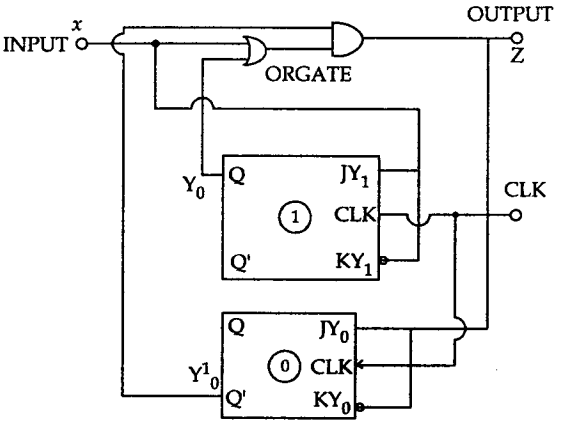
   (b) Design the circuit of four bit Amplitude comparator and explain its operation. 7

3. (a) Explain the operation of 4 bit Binary Adder-Subtractor with circuit diagram. 7

   (b) What is Binary Multiplier ? Design a combinational circuit for 2×2 multiplier. 7

4. (a) Using NAND gates, sketch a clocked RS FF. Using this FF, sketch MSJK FF and using this MSJK FF, sketch Toggle and Delay FF. 7

(b) Analyse the synchronous sequential circuit shown in figure and draw the state diagram for it. 7



5. (a) Explain the 4 bit universal shift Register using MUX. 7

(b) Design a 4 bit ripple counter using suitable waveform. 7

6. (a) What is ASM chart ? Draw an ASM chart and state table for a 2 bit up-down counter having mode control Input M = 1 :- up counting; M = 0 :- down counting. The circuit should generate an output 1 whenever count becomes minimum or maximum. 7

(b) Design a combination circuit using a ROM. The circuit accepts a 3 bit number and generates an output binary number equal to the square of the input number. 7

7. (a) With the neat diagram, Explain Dual - Slope Approximation A/D converter. 7

(b) Draw the CMOS universal gate circuit and explain its operation. 7