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CS-12

01491

ADCA / MCA (III Year)

Term-End Examination

December, 2011

CS-12 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 75*

Note : ***Question** no. **1** is **compulsory.***
*Answer **any three** questions from the rest.*

1. (a) A 150 MHz processor was used to execute a benchmar2k program with the following instruction and clock cycle counts. **9**

Instruction Type	Instruction count	Clock cycle count
Integer Arithmetic	60, 000	1
Data Transfer	40, 000	2
Floating Point	15, 000	2
Control transfer	8, 000	2

Determine the effective CPI, MIPs rate and execution time for this program.

(b) What are the factors limiting the degree of Super Scalar design ? 5

(c) What is multi - threaded processor architecture ? Explain its advantages and disadvantages in comparison to single threaded processors. 8

(d) Explain the architectural distinctions between RISC and CLSC processors. Also, explain the concept of overlapping register windows in the SPARC architecture diagrammatically. 8

2. (a) Consider the following sequence of code and answer the following questions :

$S_1 : A = D + C$

$S_2 : C = E + B$

$S_3 : D = A + C$

$S_4 : E = F + D$

$S_5 : G = E + D$

$S_6 : D = A + F$

$S_7 : B = G + T$

(i) Use Bernsteins condition to detect the maximum parallelism embedded in this code. Justify the portion that can be executed in parallel and the remaining portion that must be executed sequentially. 5

(ii) Draw a dependency graph to show all the dependences for the above code. 5

(b) Describe the differences between super - scalar and VLIW architectures in terms of hardware and software requirements. 5

3. Explain the following as applied to multiprocessors and multicomputers.
   (a) A hierarchical cache/bus architecture for designing a scalable multiprocessors. 5
   (b) Network partitioning for multicast communication. 5
   (c) Discard and Retransmission flow control. 5

4. (a) Explain the three mechanisms for instruction pipelining, giving an example for each. 9
   (b) Explain the effect of block size, set number, associativity and cache size on the performance of set associative cache organisation. 6

5. Compare and contrast the following : 15
   (a) Instruction and Trace scheduling
   (b) NUMA and COMA
   (c) Coarse gain and Medium grain parallelism