No. of Printed Pages: 3

Time: 3 hours

BIELE-015

Maximum Marks: 70

B.Tech. - VIEP - ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination June, 2015

BIELE-015: COMPUTER ARCHITECTURE

Note :		Attempt any seven questions. All questions carry equal marks. Any missing data may be suitably assumed and mentioned.	
1.	(a)	List the various register level components. Draw the generic block representation of register level components.	5
	(b)	Draw and explain in brief the internal structure of a CPU.	5
2.	(a)	Discuss the different types of instructions in an instruction set of a computer.	5
	(b)	What are the major attributes of RISC computers? State its applications.	5

J.	(a)	different fields of instruction format.	5
	(b)	Obtain the appropriate decimal value that confirms IEEE 754 floating point format for the following two numbers:	5
		(i) A = 10010111110000	
		(ii) $B = 01000111000001$	
4.	(a)	Give an adder expansion design for a 16-bit adder which is composed of 4-bit adder and linked by ripple carry propagation.	5
	(b)	Give the flow chart for Booth's algorithm suitable for signed number multiplication.	5
5.	(a)	What is the need of multilevel memory system? Briefly explain with some suitable examples.	5
	(b)	Discuss the Set Associative Mapping used in cache memory.	5
6.		do you mean by pipelining? Explain the action pipelining with the help of an ple.	. 10
7.	(a)	For two level memory hierarchy (M ₁ , M ₂),	
••	(α)	explain the following:	5
		(i) Cost and Performance	
		(ii) Hit-ratio and Miss-ratio	
		(iii) Average time of Access	
		(iv) Access-efficiency	
		(v) Space-utilization	

	(b)	Describe the general structure of Content Addressable Memory (CAM). Why is it so expensive?	5
8.	(a)	Define interrupt. Explain the different types of interrupts.	5
	(b)	Differentiate between isolated mapped I/O and memory mapped I/O.	5
9.	(a)	What is meant by program parallelism? Explain with a suitable example.	5
	(b)	Give the block diagram of DMA controller and explain its working briefly.	5
10.	Write follow	•	0
	(a)	Hardwired Control	
	(b)	Virtual Memory	
	(c)	Superscalar Processor	